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ELECTRONIC DESIGN

AUGUST 22, 1994

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FOR ENGINEERS AND ENGINEERING MANAGERS—WORLDWIDE

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STACKED CHIPS PUSH MEMORY VOLUME DENSITY TO NEW HIGHS

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- WHAT'S NEW IN INTERCONNECTIONS P. 129
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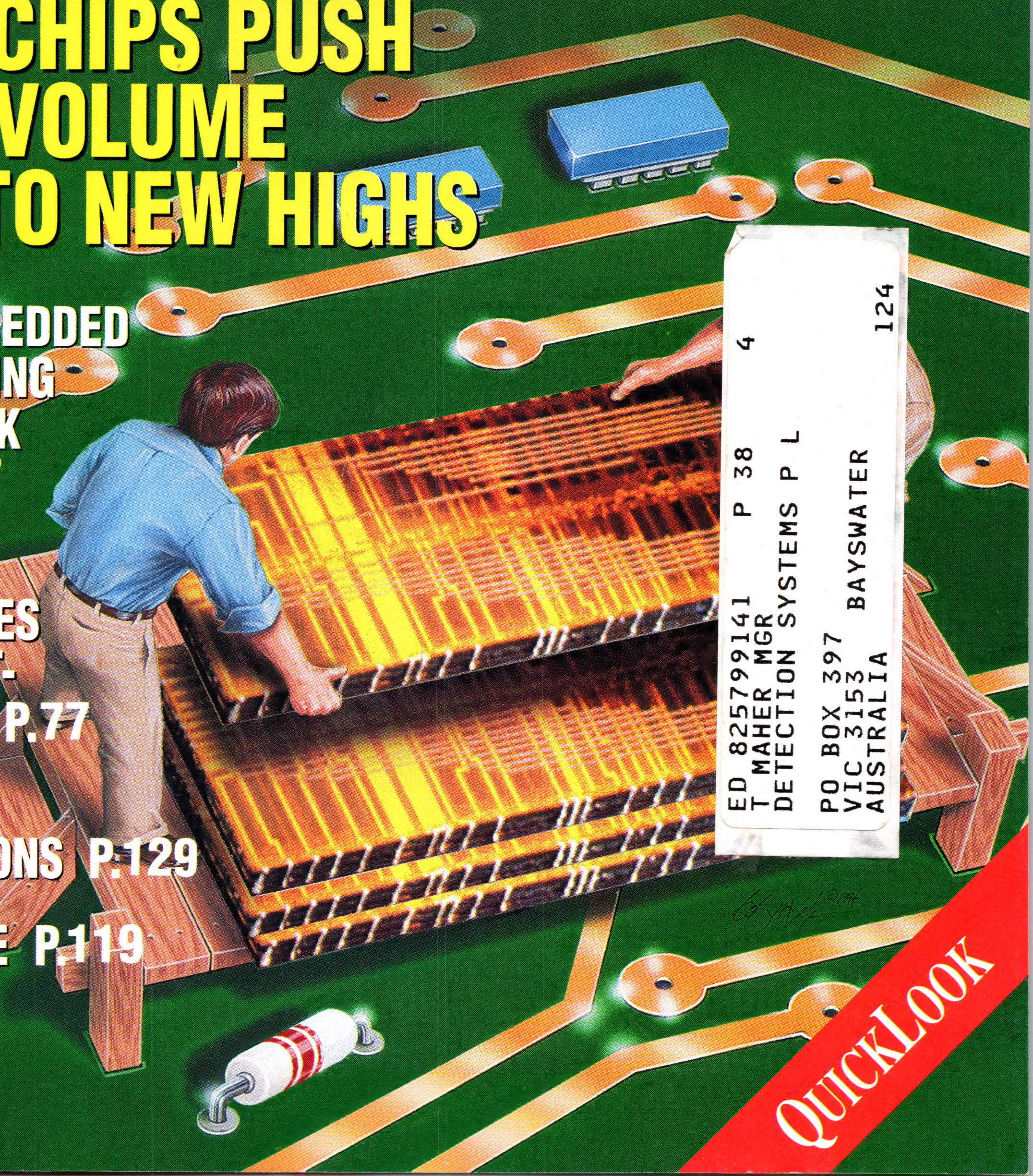

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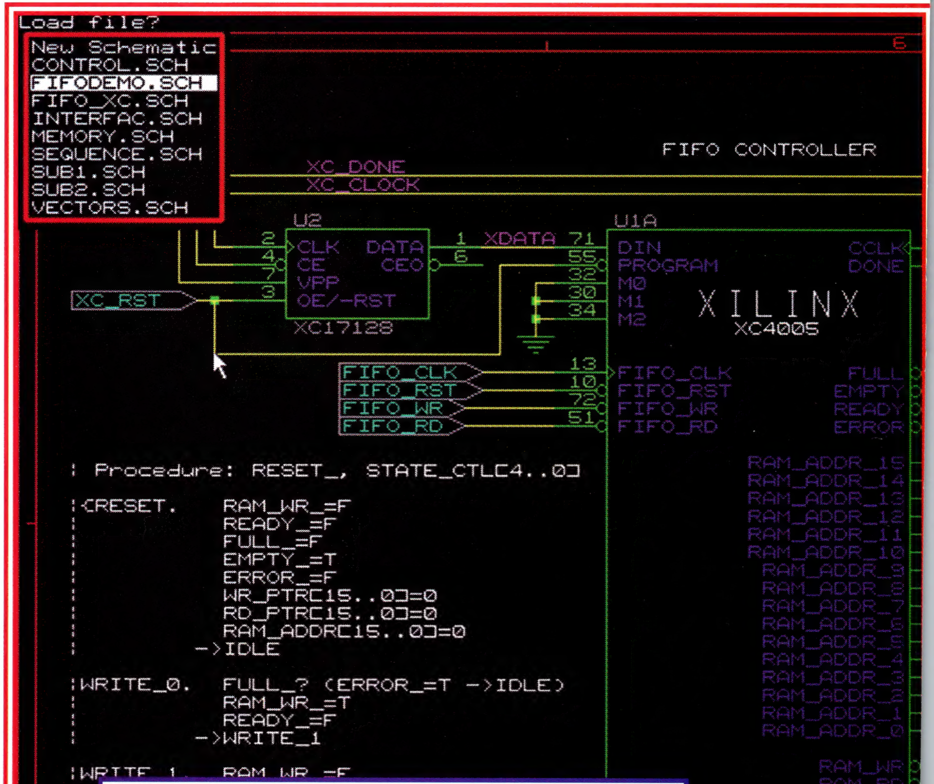
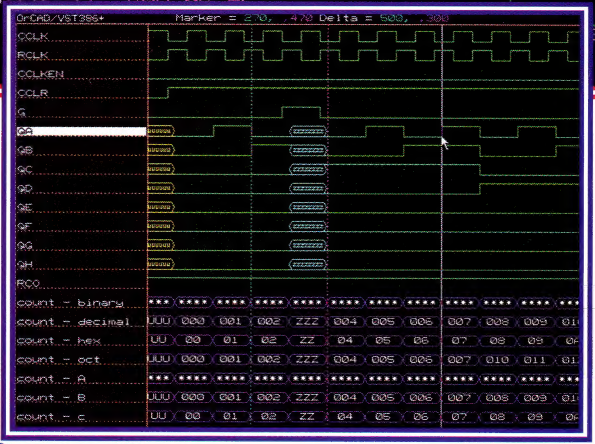


```
; Procedure: RESET_, STATE_CTL[4..0]

;<RESET.    RAM_WR_=F
;           READY_=F
;           FULL_=F
;           EMPTY_=T
;           ERROR_=F
;           WR_PTR[15..0]=0
;           RD_PTR[15..0]=0
;           RAM_ADDR[15..0]=0
;         ->IDLE

;WRITE_0.   FULL_? (ERROR_=T ->IDLE)
;           RAM_WR_=T
;           READY_=F
;         ->WRITE_1

;WRITE_1.   RAM_WR_=F
```



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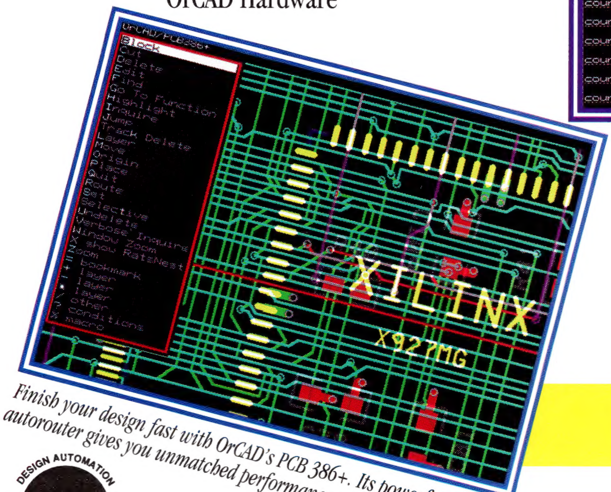

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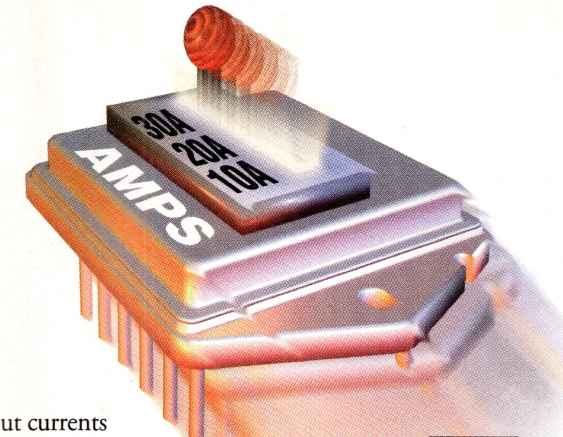
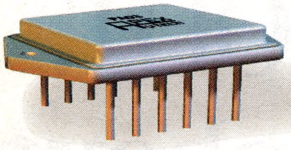
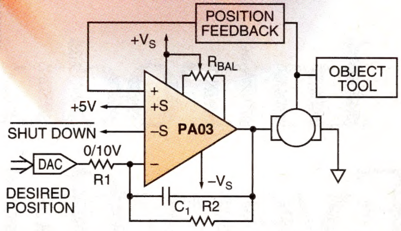


High Power, High Internal Dissipation

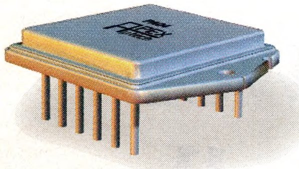


If your application requires output currents to 30A off power supplies ±15V to ±75V, take a look at the **PA03**. The **PA03** can handle up to 500W of internal power dissipation and features built-in SOA protection and external shutdown control.

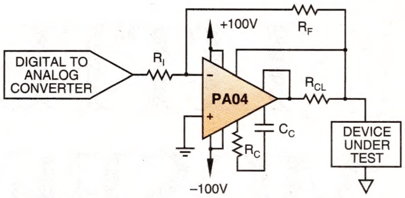


Simple Position Control Using the PA03

High Power, High Voltage

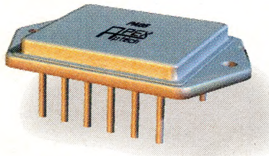


Through the extensive use of MOSFETs, the **PA04** combines 20A of output current, a wide supply range of ±15V to ±100V, 200W of internal power dissipation, and a fast 50V/µs slew rate. A power bandwidth of 90kHz rounds out the **PA04**'s impressive specs.

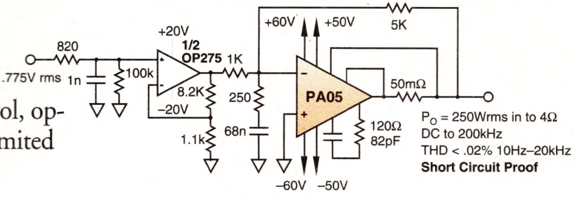


ATE Pin Driver Programmable Power Supply

High Power, High Speed



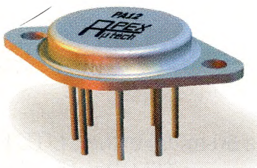
If it's speed you need, the **PA05** provides 30A of output current at a 100V/µs slew rate. The **PA05** achieves this exceptional speed on supplies from ±15V to ±50V and is capable of 250W of internal power dissipation. Its flexibility includes external shutdown control, optional boost voltage inputs and thermally limited output stages.



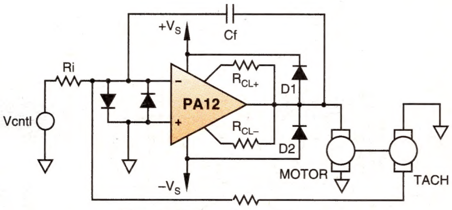
P_O = 250Wrms in to 4Ω
DC to 200kHz
THD < .02% 10Hz–20kHz
Short Circuit Proof

Premium Quality Audio Amp

High Power, Low Cost



Priced $44.70 in 1000 pieces, the **PA12** gives you versatility and value for motor/valve/actuator controls, magnetic deflection, power transducers and audio. Capable of 10A output current with current foldover protection, the PA12 works off ±10V to ±45V supplies and is capable of 125W of internal power dissipation.



Simple Motor Speed Control

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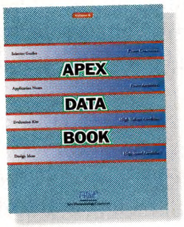

Information on all 32 of Apex's high power amplifiers is provided in the new 6th edition *Apex DC/DC Converters, Power and HV Amplifiers* data book. Call today for your free copy. **1-800-862-1021.**

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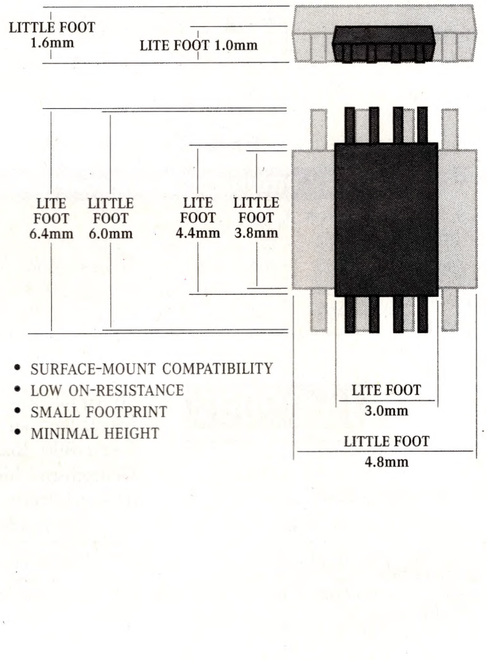

- SURFACE-MOUNT COMPATIBILITY
- LOW ON-RESISTANCE
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- MINIMAL HEIGHT

LITE FOOT™ is about half the size of LITTLE FOOT®, but delivers the same big benefits for space-sensitive and/or battery-operated applications.

Siliconix, the pioneer in 8-lead SOIC power MOSFETs, has redefined the performance of ultra-miniature, surface-mount power. The result is a new family of n-channel and p-channel devices that delivers on-resistance as low as 50 mΩ. Further, LITE FOOT features TSSOP surface-mount compatibility, and offers gate drive voltages as low as 2.7 V and currents as high as 4.2 A.

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LITE FOOT Part No.	TYPE	V_{DS} (V)	$r_{DS(on)}$ (mΩ)*	I_A (A)
Si6436DQ	Single N-Ch	30	50	4.2
Si6956DQ	Dual N-Ch	20	100	2.5
Si6433DQ	Single P-Ch	-12	75	3.5
Si6447DQ	Single P-Ch	-20	100	3.0
Si6953DQ	Dual P-Ch	-20	200	1.7
Si6542DQ	Complementary			
	N-Ch	20	100	2.5
	P-Ch	-20	200	1.7

* On-Resistance shown at V_{GS} = 10 V, except Si6433DQ shown at V_{GS} = 4.5 V

MOSFET thin enough to fit into any standard PCMCIA card. Even double-sided circuit boards are a snap.

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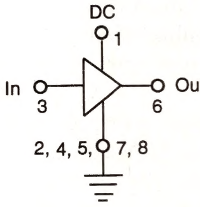

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Max. Output (dBm) @1dB Comp. typ.	+18.0	+18.5	+17.5	+17.0
I P 3rd Order (dBm) typ.	+27	+27	+27	+27
VSWR Output typ.	1.5:1	1.7:1	1.7:1	1.5:1
VSWR Input typ.	6.4:1	2.8:1	2.0:1	1.4:1

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AUGUST 22, 1994 VOL. 42, NO. 17

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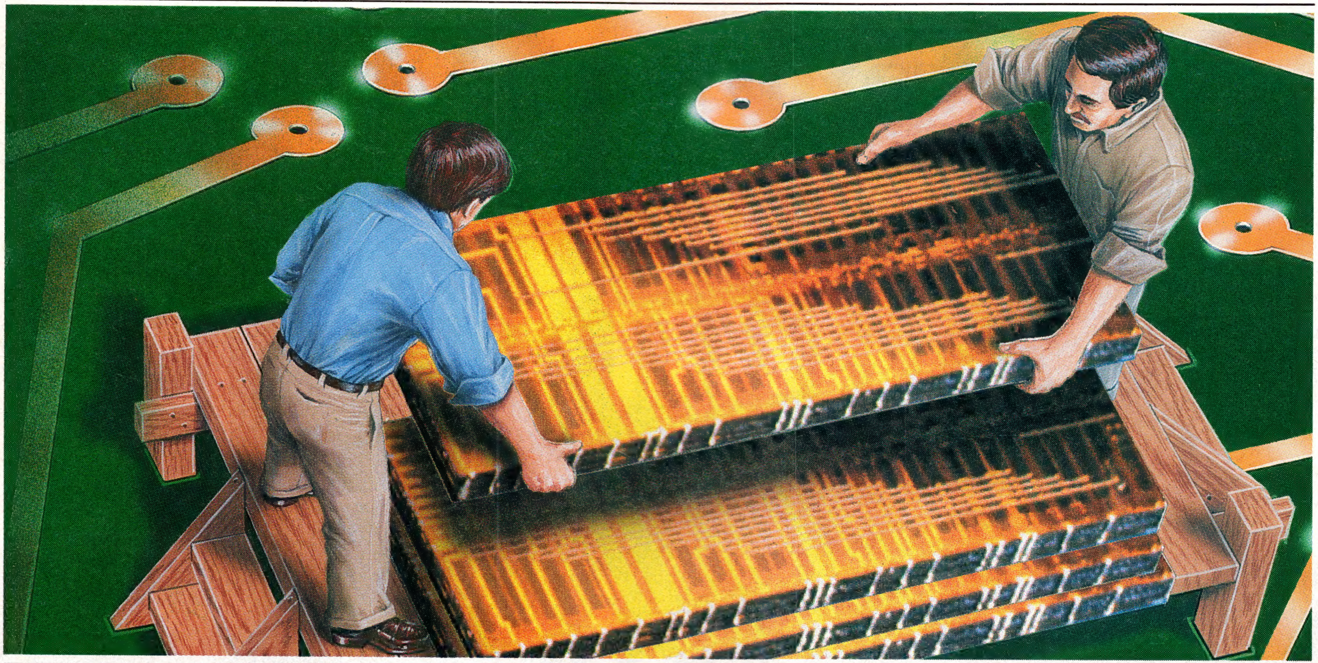

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1968 First Place Award
1972 Certificate of Merit
1975 Two Certificates of Merit
1976 Certificate of Merit
1978 Certificate of Merit
1980 Certificate of Merit
1986 First Place Award
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- Tips on designing battery-backup and watchdog circuits
- GaAs challenge renewed for high-speed communications applications
- Technologies catapult PCMCIA hard-drives to new capacity heights
- PLUS:

Pease Porridge
Ideas for Design
QuickLook

Correction: The sidebar on pg. 64 in the June 13 issue inadvertently referred to the new TIA standard for TDMA digital cellular transmissions as IS-94. Instead, it should be IS-54.

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ELECTRONIC DESIGN 40 YEARS AGO

Analog-Digital Converter For Data Handling Systems, Computers

This component simplifies and speeds up analog-digital conversion by eliminating ambiguity and intermediate analog steps in the conversion process. The signal travels from shaft position to code disks and then to either a relay system or a diode scanning network followed by a single flip-flop. Time sharing of control circuits is possible for multi-channel systems, using isolation diodes in series with each pick-off brush, allowing the control circuit to be used for scanning many converters. Ambiguity is eliminated by using two pick-off brushes for each track of the code disk except the first, or least significant. Standard code disks are made for binary operation, but Gray, decimal, or other systems may be ordered. Present models include 7, 13, 17, and 19 digit units, all 2" in diameter and varying from 2-49/64" to 4-13/16" in length. Conversion from digital code to analog shaft rotation may be made with a slight increase in circuitry.

Input torque is under 0.2 oz-in. Current carrying capacity is 2ma per pick-off brush. Digit output frequency may vary from 500cy to 1Mc or higher. The unit operates independent of voltage, temperature, and frequency limitations over a wide range. Life expectancy is 5,000,000 or more cyclings of input shaft at speeds 1-2rps. Weight is 8oz. Librascope, Inc., 1607 Flower St., Glendale, Calif.*(Electronic Design, August 1954, p. 58.)*

These types of rotary ADCs once were widely used at the heart of many data-acquisition systems. They still are used today in robotic systems and the like to convert angular position to digital code. The Gray-code format mentioned in the item is often used because it has the property of changing only one bit for each successive integer, thus avoiding ambiguous states as the device switches from one integer to another.—SS

AEC Patents For Industry

Patents owned by the Atomic Energy Commission have been made available for licensing. Licenses will be granted to applicants on a non-exclusive, royalty-free basis. Applicants should apply to the Chief, Patent Bank, Office of the General Counsel, U.S. Atomic Energy Commission, Washington 25, D.C., identifying the subject matter by patent number and title.

Electronic Scaling Circuits (Patent No. 2,676,756); M. Q. Gulley, inventor. The patent relates to an improvement for modifying the counter factor of a scaling circuit. The invention is capable of the modification of any suitable conventional scaling circuit to make it count in multiples of 10 or other convenient multiples.*(Electronic Design, August 1954, p. 75.)*

This is one of several AEC patents listed in the issue. Many improvements in high-speed counting equipment came out of the atomic-energy programs.—SS

Atomic-electronic guard

Radioactive leather wristbands worn by a power-press operator prevent accidents by activating an electronically operated machine lock driven by a Geiger tube whenever he places his hands near a cutting edge. Nicknamed "Bikini Bracelets," the wristbands are not dangerous to the wearer. For complete safety, the Geiger tubes (mounted on the press) are sensitive enough to detect when the operator has removed the band, preventing the press from operating. This protective system, already widely used, is made by Hazatrol Corp., San Francisco, Calif.*(Electronic Design, August 1954, p. 11.)*

Radioactive bracelets that "are not dangerous to the wearer"? This item seems tough to believe from the perspective of today's OSHA-sensitive working environments.—SS

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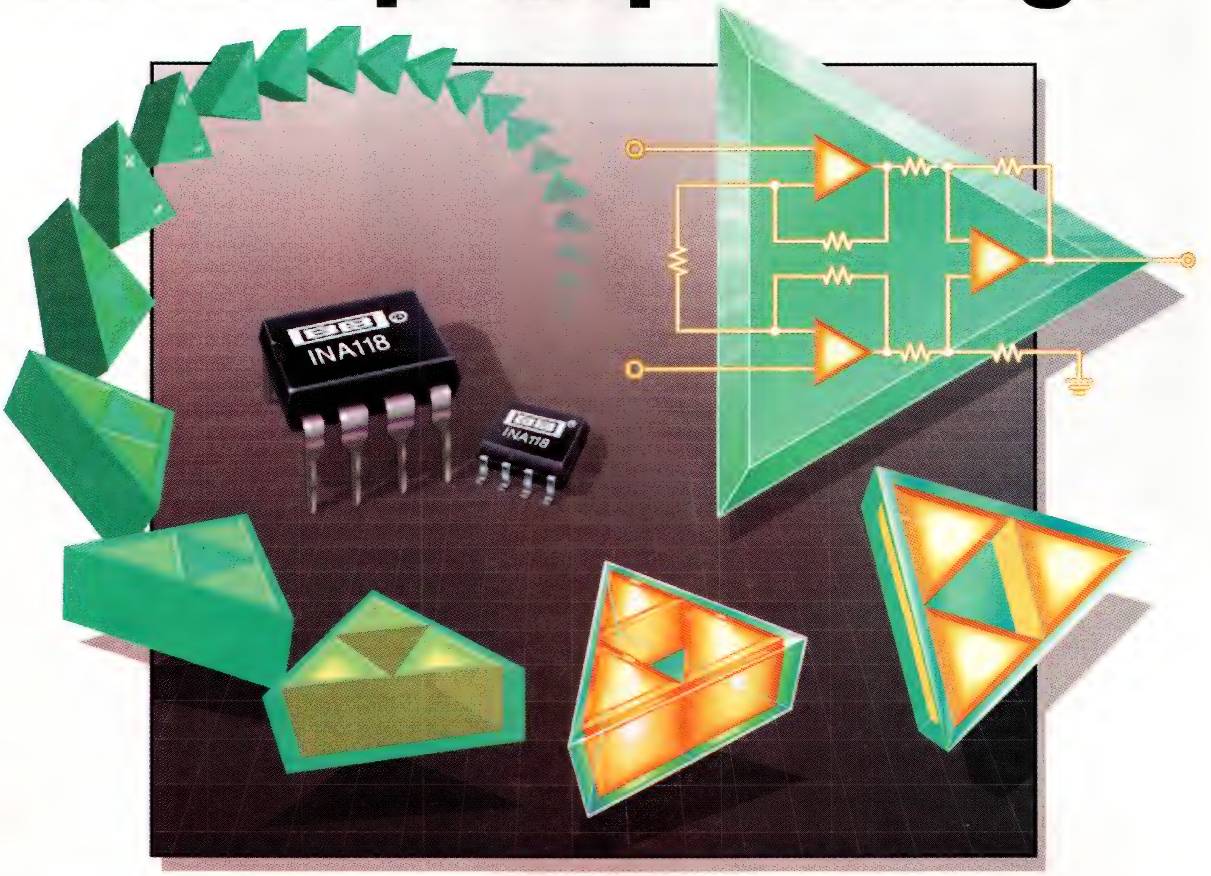

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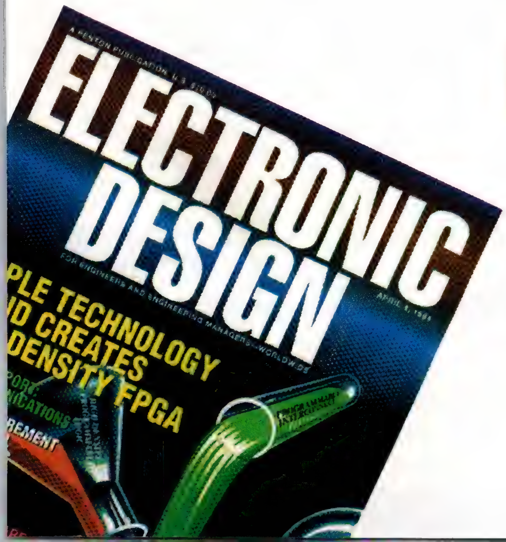

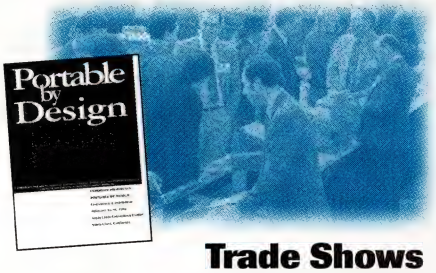

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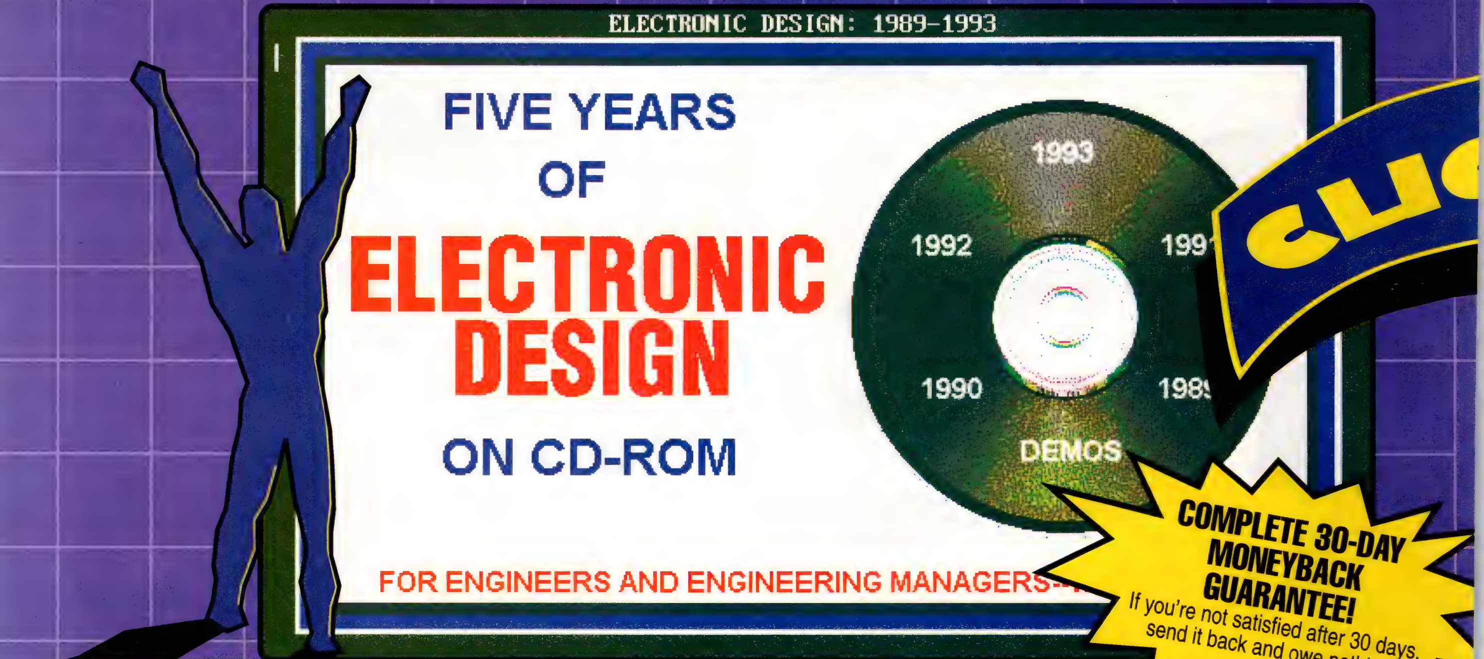
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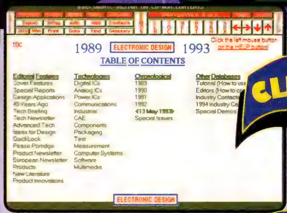

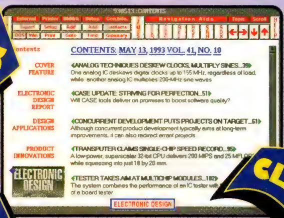

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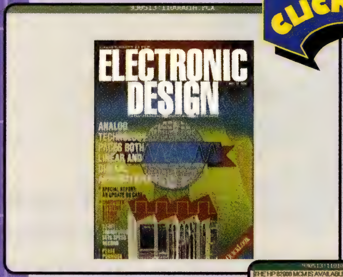

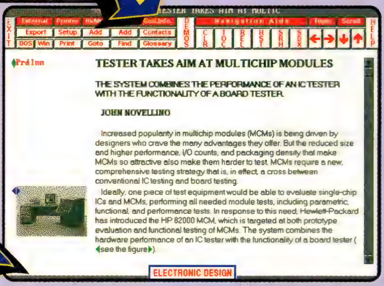

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JOHN NOVELLINO

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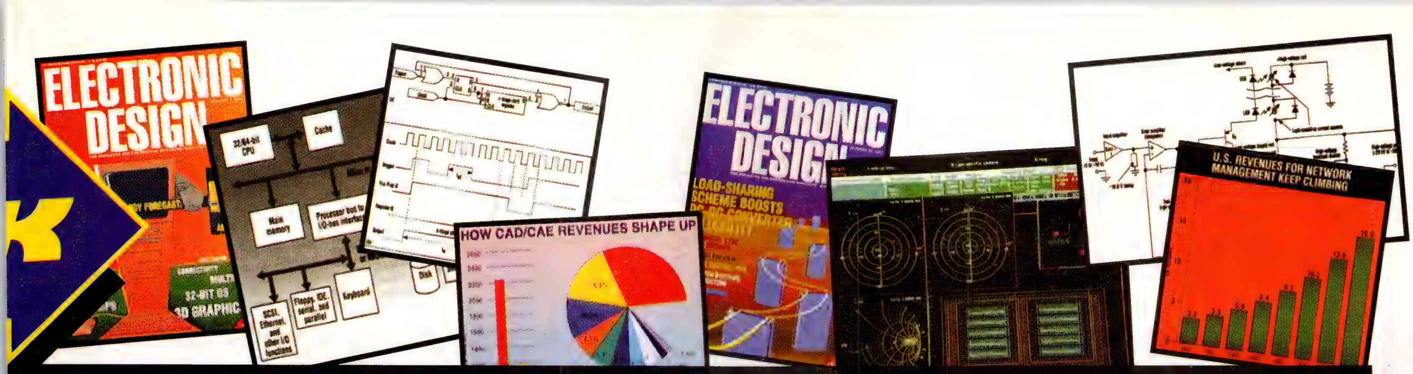
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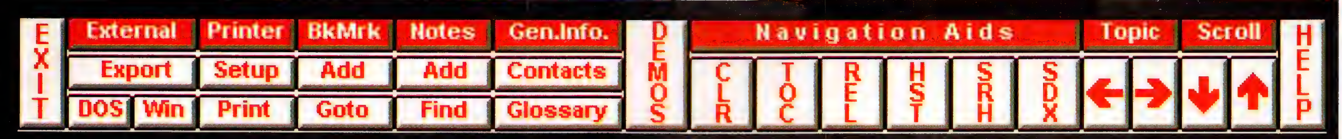

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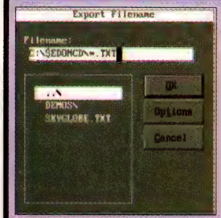

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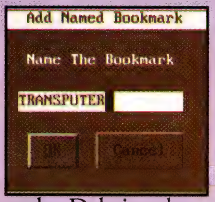

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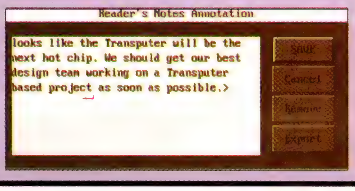

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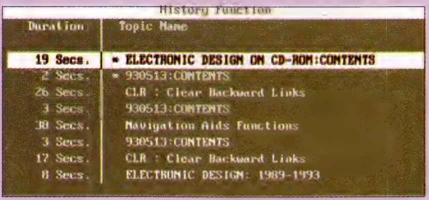

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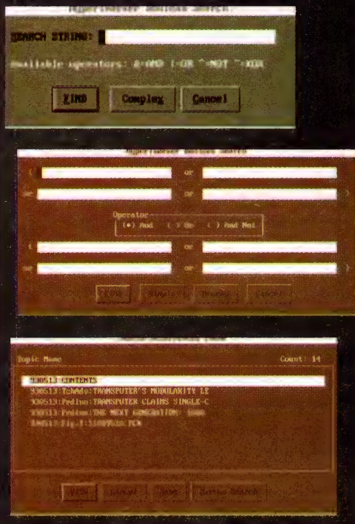

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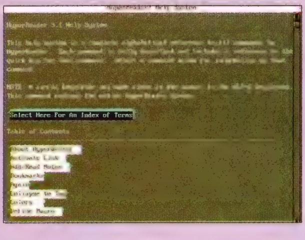

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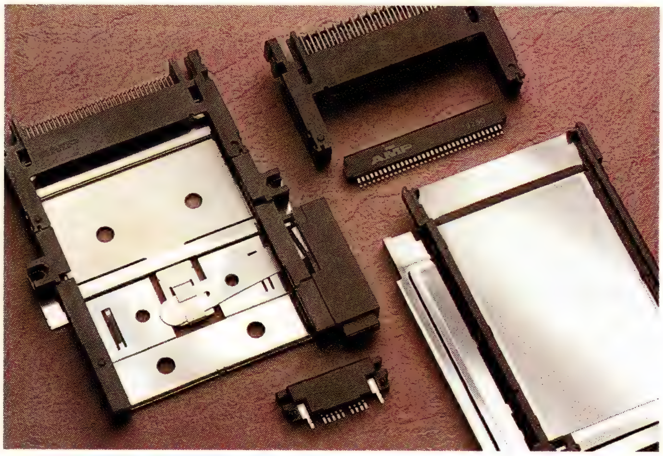

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STOCK OPTIONS

What, you might ask, is an editorial about stock options doing in a magazine devoted to delivering information about electronics? The answer is that one of the driving forces behind technology development in the United States is stock options. Obviously, without healthy doses of innovation, the industry would stagnate and we journalists would be reduced to mastering Mine Sweeper and other mindless games on our PCs.

The biggest financial carrot that helps small, startup companies entice top-notch people from high-paying jobs at large companies is to offer the prospective employee a piece of the company. Needless to say, these small companies are the cradle of much innovation—not to mention jobs—in our industry.

A few months ago, a rather obscure government agency, the Financial Accounting Standards Board (FASB), proposed change in accounting practices that threatened to decimate innovation in any U.S. high-tech industry. FASB's proposal would require companies to calculate values for employee stock options—a highly speculative exercise to say the least. These figures then would be charged as an expense on the company's financial statements.

A survey conducted by ShareData Inc. earlier this year found that of 30 high-tech companies studied, the average reduction in earnings would be 29%. That's far from an insignificant figure for any company.

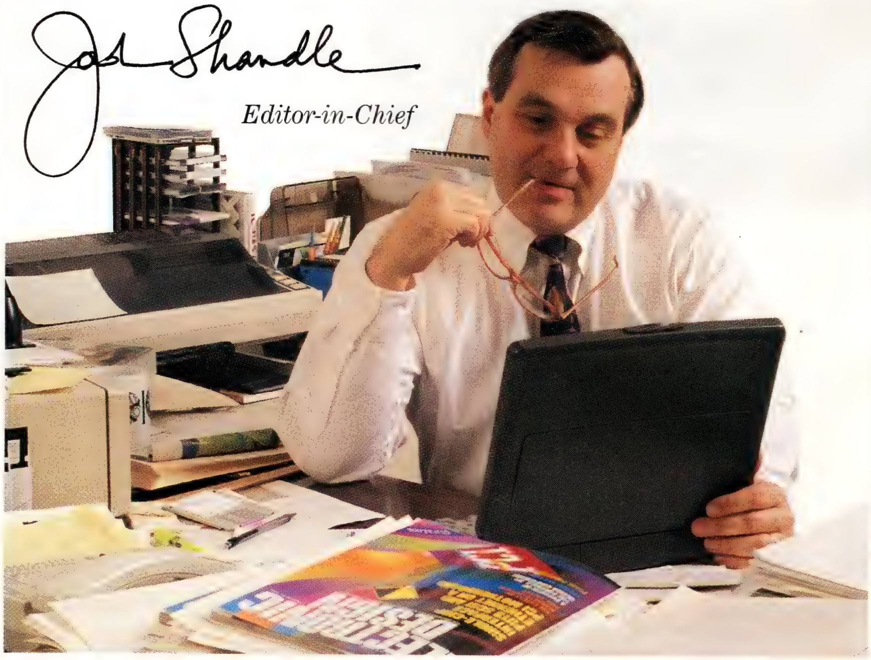
Last June, FASB's rule change was met with an uncharacteristic response from the electronic-engineering community. The response was both unified and vociferous in its opposition. Even industry maverick T.J. Rodgers, president of Cypress Semiconductor Inc., found himself in the majority on this one. "Our earnings would collapse by 33%," he said at a Silicon Valley anti-FASB rally, "and you know what that means on Wall Street where even one bad quarter carries a severe penalty."

FASB has taken note of the tidal wave of opposition. The Board postponed its decision until 1995 and indicated it might settle for a more detailed accounting of stock options. This remedy is widely supported by high-tech companies and would effectively address the real problem with stock options, which is making them into a golden parachute for executives.

But some folks, like me, think the bureaucrats might be lying in the grass for awhile until the opposition dies down. Let's keep the pressure on.

Josh Shandle

Editor-in-Chief



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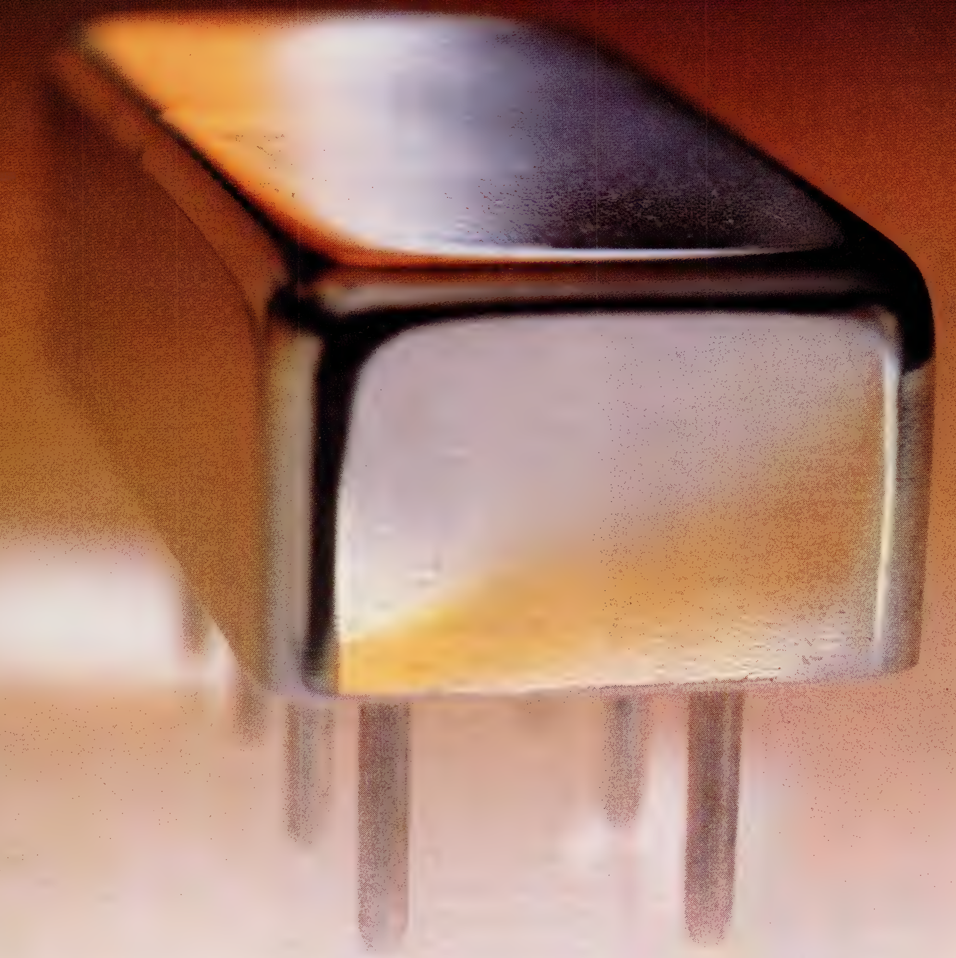

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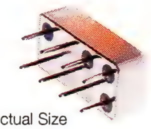

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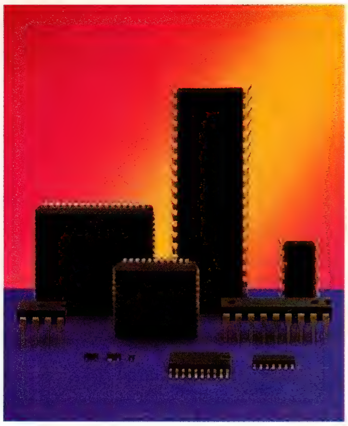

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ASIC VENDORS LOOKING FOR TEST HELP

The increasing amount of ASIC designs for devices exceeding 50,000 and even 100,000 gates makes the job of creating test programs for such circuits a virtual nightmare. ASIC vendors have taken notice, however, and are searching for ways to cut the time it takes to develop a test, with improved test vectors from the design team being a critical element.

From their point of view, the vendors promise to turn the design team's efforts into silicon within a specified time. Too often, the vectors supplied by the team don't work. They may not match the specific tester used by the vendor or they may be riddled with timing gymnastics that no tester can keep up with. If it takes a week or two to find the problems and generate new vectors, which it easily can, the vendor is squeezed to meet its promised delivery date.

The result is an effort by vendors to encourage designers to come up with better vectors. "We're seeing ASIC vendors being much more concerned about trying to screen test programs before the vendors ever get the design. In other words, on the customer's time," says Daniel Skilken, senior vice president of worldwide marketing for Summit Design Inc. (formerly TSSI), Beaverton, Ore. "It's a matter of, 'You give me a clean design and you give me a clean set of vectors and I know that I can deliver when I said I could.' "

In fact, two ASIC vendors have talked to Summit about including the company's software for screening test programs in the vendors' design kits. Skilken says the vendors use the software in-house but want their customers to start using it on the test programs before they're sent to the foundry. One vendor that solved the problem is Semicustom Operations in Motorola's High-Performance Microprocessor Div., Chandler, Ariz. The unit includes Summit's TDS software in its design kit to ensure that the test vectors created from the customer's simulation vectors will work.

JOHN NOVELLINO
TEST & MEASUREMENT

Lynn Fischer, a member of the technical staff at Semicustom Operations, introduced the practice. He came from a Motorola research lab that received test patterns from numerous customers. "We had many problems with the patterns," says Fischer. "They would give us patterns that wouldn't work and we'd have to sit down and more or less let a customer just walk through it."

Semicustom Operations wrote software that envelops the Summit toolset and runs in the background. Designers enter their simulation and the tools check to make sure that the timing is as required. They also do a rules check, help designers determine where to put strobe points, and make sure that the patterns toggle all of the outputs. The software has been such a success that it is being modified so that other groups within the division can use it.

Another vendor, LSI Logic Corp., Milpitas, Calif., integrates vector and test program creation into the company's design methodology. In that way a proper test program is essentially generated as part of the design process. "We explain to customers the right approach to generating test vectors so they don't cause holdups," says Farzad Zarrinfar, product marketing manager for Test Synthesis Solutions. "We have a really clear set of methodology guidelines for designers to use to simulate their designs."

The company's first line of defense against bad vectors is a network of design centers where ASIC experts review the process of design simulation with customers. Then comes an automated toolset that performs rule checking to make sure the simulation vectors conform to the design process. By using the proper design methodology and CAD tools, Zarrinfar says, designers can ensure that their simulation vectors will not cause any problems.

The bottom line is that foundries expect design teams to supply better test vectors, vectors that will not violate the limits of the equipment used to test the ICs. Fortunately, they're willing to help designers accomplish that goal.

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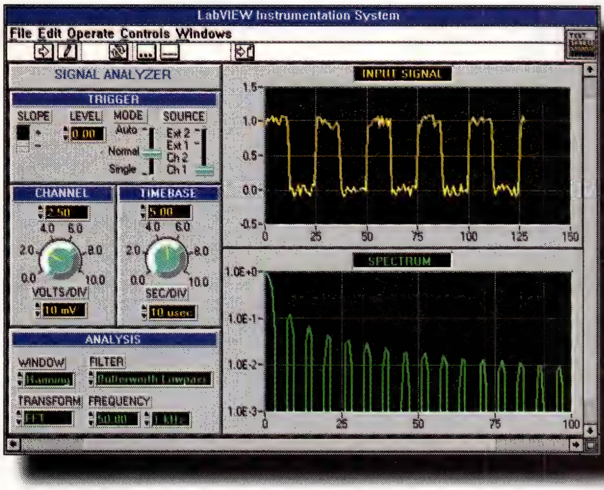

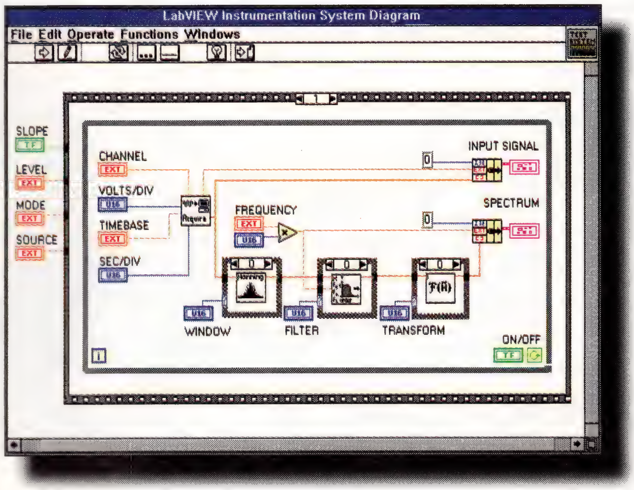

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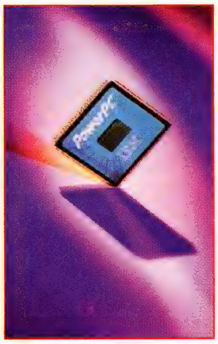

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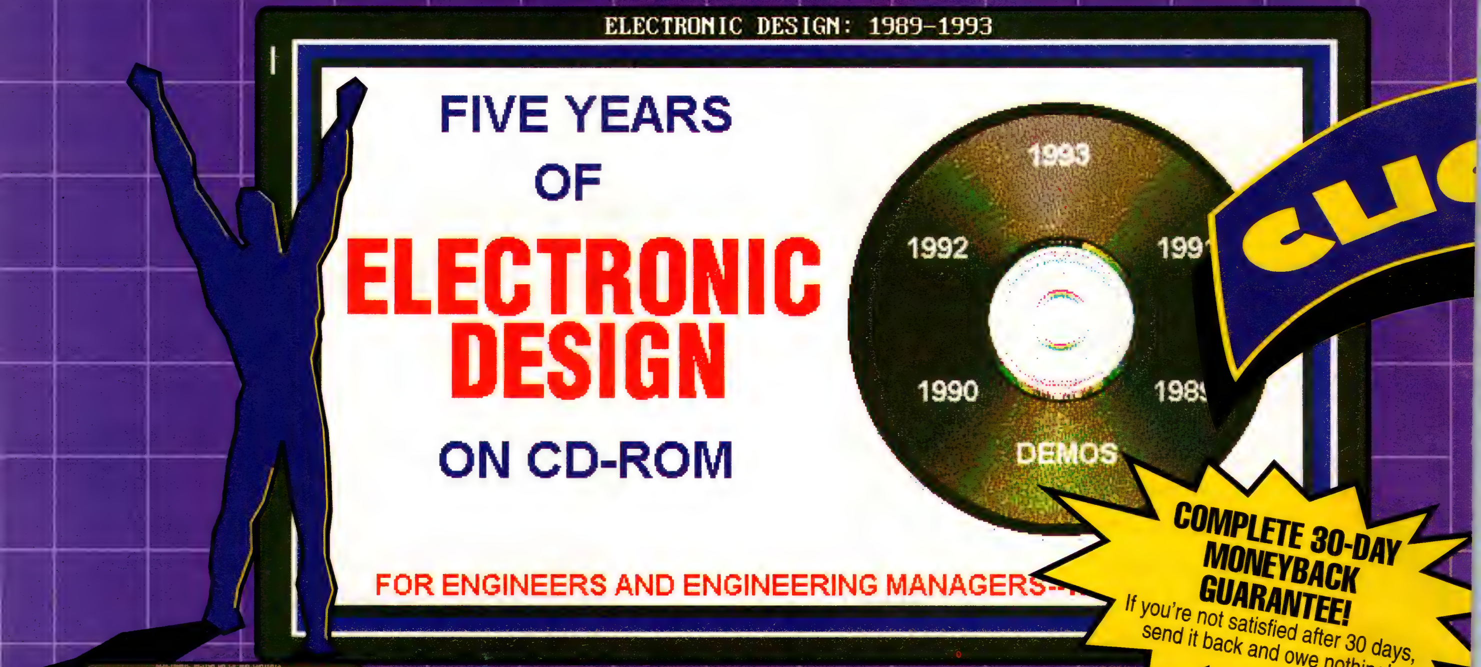
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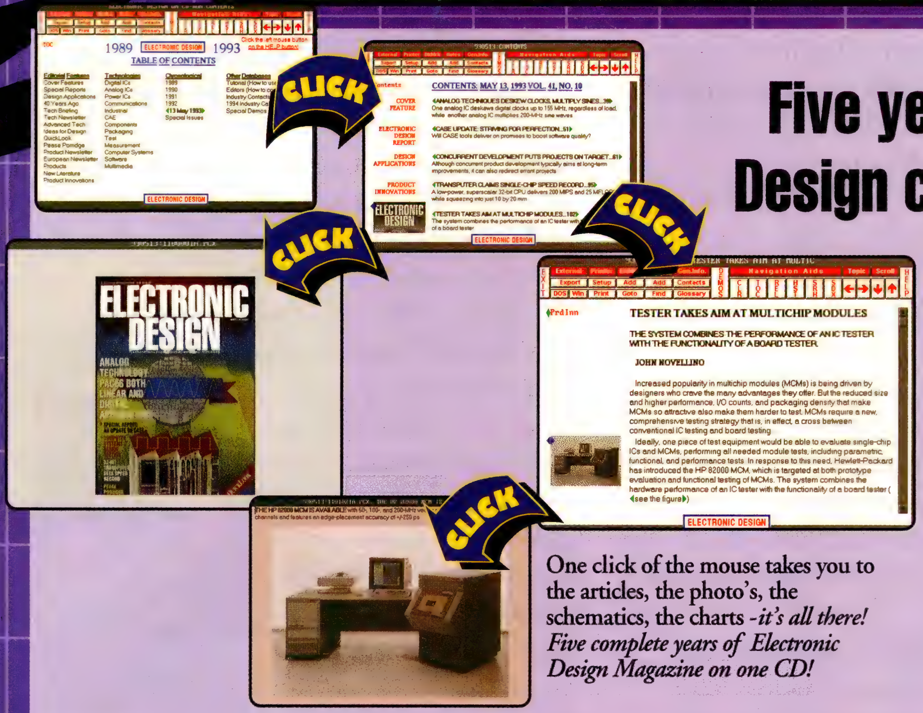

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TESTER TAKES AIM AT MULTICHIP MODULES

THE SYSTEM COMBINES THE PERFORMANCE OF AN IC TESTER WITH THE FUNCTIONALITY OF A BOARD TESTER.

JOHN NOVELLINO

Increased popularity in multichip modules (MCMs) is being driven by designers who crave the many advantages they offer. But the reduced size and higher performance, I/O counts, and packaging density that make MCMs so attractive also make them harder to test. MCMs require a new, comprehensive testing strategy that is, in effect, a cross between conventional IC testing and board testing.

Ideally, one piece of test equipment would be able to evaluate single-chip ICs and MCMs, performing all needed module tests, including parametric, functional, and performance tests. In response to this need, Hewlett-Packard has introduced the HP 82000 MCM, which is targeted at both prototype evaluation and functional testing of MCMs. The system combines the hardware performance of an IC tester with the functionality of a board tester (see the figure)

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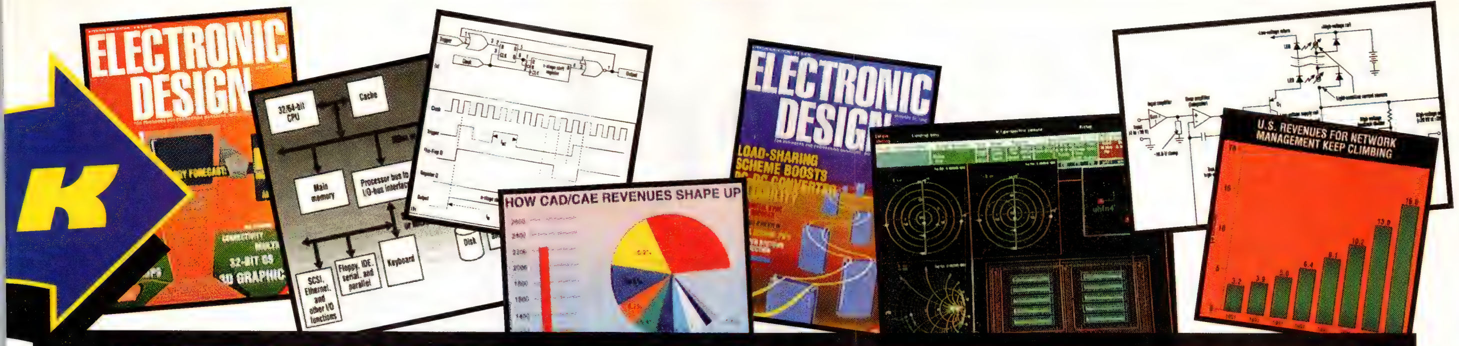
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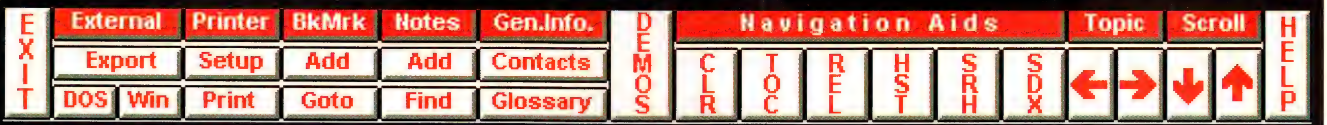

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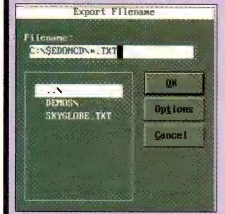

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The **Export** button will export any or all of an article based on your selection.

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DOS brings you to the DOS prompt screen and **Win** takes you into Windows™ without quitting the application. These buttons make it easy for you to return to Electronic Design Magazine, where you left off, without re-launching.

Printer Commands

Setup & **Print** - This feature allows you to print articles, editorials, glossaries, illustrations, and even photos *(if your printer is capable)* directly from this CD. Great source for reference.

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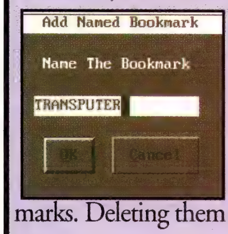

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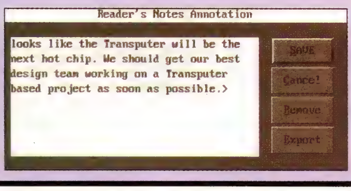

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Reader's Notes Annotation
looks like the Transputer will be the
next hot chip. We should get our best
design team working on a Transputer
based project as soon as possible.>
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Gen. Info - Complete reference

Contacts - Company names, addresses, contact names, phone numbers- all of the information you need to follow up.

Glossary - Full article glossaries, provided by the Editors of Electronic Design magazine. The CD also comes with WORD LINK, which allows you to click on any word within the article and if it's in the glossary, the definition pops up. When you're done, a simple click and it's gone.

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CLR - *Clear Back Links* - Because every article you move to loads into RAM, this function allows you to clear articles you've finished. This frees up RAM for you to continue.

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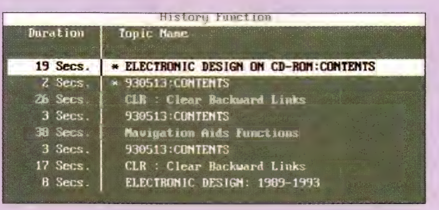

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                    History Function
 Duration   Topic Name

 19 Secs.   * ELECTRONIC DESIGN ON CD-ROM:CONTENTS
  2 Secs.   * 930513:CONTENTS
 26 Secs.     CLR : Clear Backward Links
  3 Secs.     930513:CONTENTS
 38 Secs.     Navigation Aids Functions
  3 Secs.     930513:CONTENTS
 17 Secs.     CLR : Clear Backward Links
  8 Secs.     ELECTRONIC DESIGN: 1989-1993
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REL - *Show-Related Articles* - Calls up a list of, and lets you move to, related topics.

HST - *Show-Related History* - Shows each topic visited during your current session and how long you were there, and then lets you return to previous topics.

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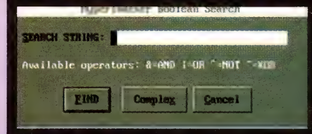
Simple search (top), Complex Search (center), and Search occurances found (bottom).



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Boolean Search
SEARCH STRING:
Available operators: &=AND |=OR ^=NOT ~=XOR
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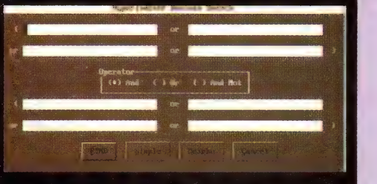

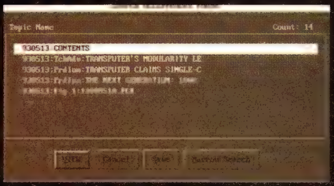

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Topic Name                                Count: 14
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930513:TeWdw:TRANSPUTER'S MODULARITY LE
930513:Prdlow:TRANSPUTER CLAIMS SINGLE-C
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SRH - *Search* - Conduct simple, complex or proximity indexed searches.

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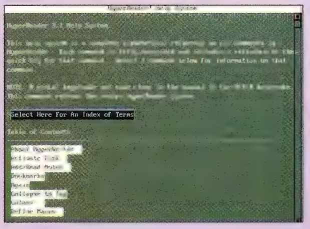

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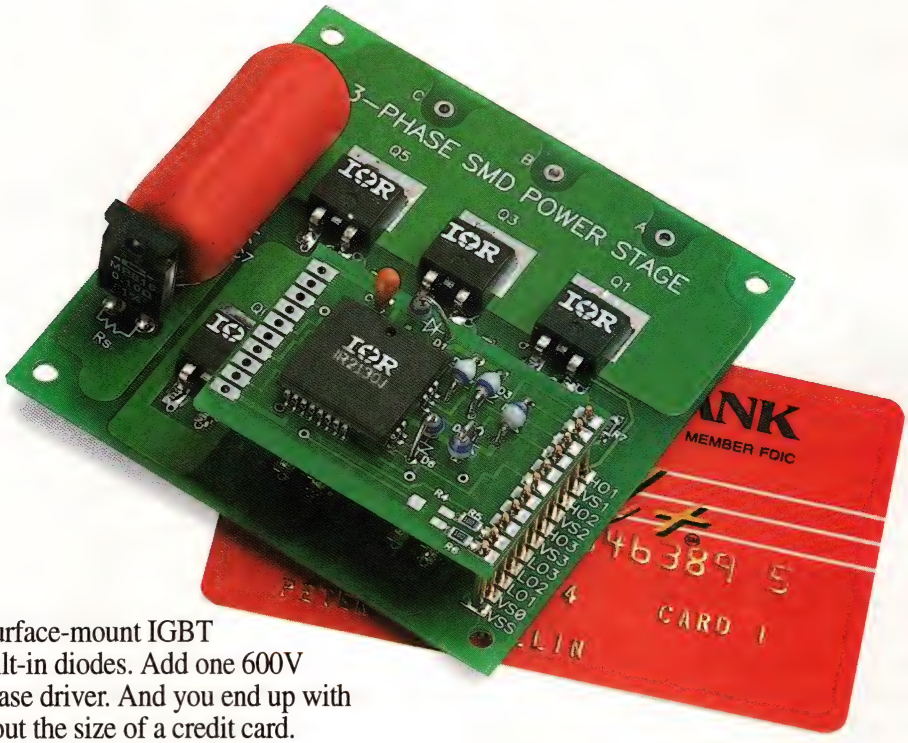

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TECHNOLOGY NEWSLETTER

PCS STANDARDS, CELLULAR-PCS BRIDGE UNVEILED

The Telecommunications Industry Association has published two interim standards to provide guidance for developers involved with Personal Communications Services (PCS) products. The first document, "Personal communications service descriptions for 1800 MHz," identifies those PCS services that should be standardized in all PCS systems and specifies operation of those services. This interim standard, listed as TIA/EIA/IS-104, is now available. Products built to this standard will enable PCS subscribers to use any PCS device to access the services of any system with a uniform PCS unit-to-network interface. The second, EIA/TIA/IS-94, is entitled "Mobile station-land station compatibility specifications for analog cellular auxiliary personal communications service." This interim specification provides the minimum specs for an air interface that will support "closed user groups," (groups of PCS units with limited geographic capability within a macrocellular service area). The document also provides an air interface specification that allows 800-MHz cellular service to be delivered to a closed user group. The technical requirements contained in the document form a compatibility standard for Cellular-band Auxiliary Personal Communications Systems (CPACS), which assures that all CPACS equipment is interoperable. Reprints of these documents are available through Global Engineering Documents for $110 for IS-104, and $93 for IS-94. Call Global at (800) 854-7179. *LG*

FPD INSPECTION TOOLS IMPROVE DISPLAY QUALITY

With much attention focused on the display industry—especially in light of the $600 million, five-year subsidy for flat-panel display manufacturing promised by the current administration—it's become increasingly important to guarantee the quality of display products. Because each screen is made on a large glass substrate, potentially measuring up to 18 in. or more in dimension, a small error in manufacturing could render an entire screen unusable. To this end, a full line of instruments for high-performance inspection were developed by the Instrument Group of Nikon, Melville, N.Y. One product is an XD-20 microscope that can handle substrates 18 in.^{2}. The instrument consists of a series of chromatic aberration-free objectives, and has fully automated operations, ergonomic features, contaminant-free design, and rigid construction. Another instrument, the Optiphot 300 handles liquid-crystal displays, as well as large semiconductor wafers. It is equipped with a massive cantilevered arm, making it possible to accommodate samples up to 300 mm in diameter. It is believed that these instruments will effectively contribute to the cost-effective production of high-quality displays through accurate, clean, repeatable, and fast inspection techniques. For more information, contact Nikon at (516) 547-8531. *CA*

SOON TO ARRIVE: FPD CLUSTER TOOLS

As part of a $1.7-million program, under the sponsorship of the U.S. Display Consortium, San Jose, Calif., Accudyne Corp., Palm Bay, Fla., will attempt to produce cluster tools for automating the application of spacers in flat-panel-display manufacturing. This application is crucial because the uniform spacing between the top and bottom glass plates required for liquid crystal displays is essential to achieving proper optical performance. Many U.S. manufacturers have been left on their own to develop equipment specifically focused on this process step. Unfortunately, their efforts have met with great expense and unsatisfactory results. Accudyne's system will help to alleviate this problem by developing a fully integrated and automated system that can clean glass, apply spacers, and verify all process results. The project should be completed by July, 1995. Call Accudyne Corporation at (407) 724-6500. *CA*

NIST IMPROVES OPTICAL POWER-METER CALIBRATION

A new method for calibrating optical power meters uses tunable laser diodes to calibrate the meters at either a specific wavelength or over the range of wavelengths of the tunable diode. The technique, developed by the National Institute of Standards and Technology, Boulder, Colo., is an addition to the existing method NIST has used for some time to calibrate optical power meters at fixed wavelengths, using both collimated beam and fiber/connector configurations. Installation of the tunable laser diodes in the measurement system minimizes the errors associated with the source wavelength and detector spectral responsivity. The new technique is explained in a paper titled, "Optical power meter calibration using tunable laser diodes," by Igor Vayshenker, Xiaoyu Li, and Thomas R. Scott. Contact Sarabeth Moynihan, (303) 497-7765. *JN*

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STANDARD LINKS INCREASE FUTUREBUS+ PERFORMANCE

By complying with the IEEE 896.11 standard, systems will be able to employ low-cost IEEE 1355 standard links to add up to an order of magnitude to the performance of the Futurebus+ backplane. The standard, called IEEE 1355 Links on Futurebus+ Backplane Connector, retain all of the Futurebus+ performance and interoperability benefits. The standard is aimed at a broad range of applications, including ATM, graphics supercomputers, workstations, massively parallel supercomputers, disk arrays, and mainframes. The standard supplies point-to-point bandwidth for interworking Futurebus+ card from different originators. Up to 16 links per enhanced slot can be employed, all supporting a bidirectional bandwidth between a Futurebus+ card and the backplane in excess of 1 Gbyte/s. The standard will have no effect on the use of current standard Futurebus+ interfaces. For more information on the IEEE P896.11 standard or the P1355 Working Group, contact Dr. Colin Whitby-Strevens of SGS-Thomson/Inmos Ltd. in the U.K. at +44 454 611500. He can also be reached at electronic-mail address colinws@isnet.inmos.co.uk. *RN*

VIRTUAL REALITY TESTBED TAKES WING

Because virtual reality enables users to interact with a simulated environment as if it were real, among its applications is the ability to practice jobs that are too dangerous or expensive to carry out for real. To further development of virtual reality (VR), NIST's Computer Systems Laboratory in Gaithersburg, Md., has established an Open Virtual Reality Testbed, which includes prototype VR systems. The testbed was set up to encourage development of standard interfaces for interoperability of VR components from different vendors. Information and sample demonstrations of testbed activities are available online at http://nemo.ncsl.nist.gov/~sressler/OVRThome.html. For more information, contact Sandy Ressler (301) 975-3549. *SVT*

TOOL RESEARCH TARGETS QUASI-OPTICAL SYSTEMS

Through the help of a Small Business Innovative Research grant, Compact Software, Paterson, N.J., will work to create CAD tools that support the design of quasi-optical microwave applications. Compact has teamed up with Avoca Labs and Cornell University to develop a planar, high-power, quasi-optical amplifier array. The array is based on successful experimentation work done at Cornell through Raytheon support. The design is based on series of unit-cell monolithic power amplifiers isolated from each other in such a way that they can be modeled and evaluated individually with relative ease. During Phase I of the grant, Compact will develop software tools to accurately simulate the components of the quasi-optical system. Such a capability doesn't exist in current commercial simulation tools, and is considered to be an obstacle in exploring new ideas in this emerging field. During Phase II of the grant, an amplifier array (composed of 20-by-20 cells) will be designed and optimized using Compact's commercially available nonlinear circuit simulator called Microwave Harmonica. The amplifier array will then be built using advanced GaAs technology. Compact will also develop simulation tools to enable modeling of grating patterns for instances of non-normal incident radiation. For more information, call Compact Software's Todd Westerhoff at (201) 881-1200. *LM*

CHEMICAL SENSOR BOASTS SUPER SENSITIVITY

A chemical sensor calorimeter recently developed and introduced by the IBM Research Division's Zurich Research Laboratory, Zurich, Switzerland, is capable of measuring the heat generated in a chemical reaction with a sensitivity to temperature changes as small as one-hundred-thousandth of a degree. Microfabricated using IC technology, the calorimeter is inexpensive, making it ideal for a variety of applications, including chemical observation, detection, measurement, and analysis. The calorimeter centers around the use of an aluminum-coated micromechanical silicon lever. The lever is approximately 1.5 μm in diameter, and 400 μm long, allowing for possibly thousands of such levers to be integrated on a single chip. As the calorimeter heats, the two materials, silicon and aluminum, expand by different amounts causing the lever to bend. The amount of bending directly relates to the amount of heat that has been absorbed by the lever. Using a laser to measure this amount of bending, bends as small as one hundredth of the diameter of an atom can be measured. Using this technique, levers could be coated and sensitized for the detection of very specific chemicals. Scientists believe that the calorimeter could be incorporated into a portable package with a laptop computer to create an instrument capable of detecting gases and pollutants, such as ozone and carbon monoxide. Future research will focus on the use of micromechanics and nanotechnology to make the already sensitive calorimeter thousands of times even more sensitive. For additional information, contact IBM Research Division at (914) 784-7466. *CA*

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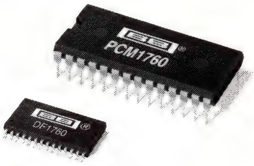

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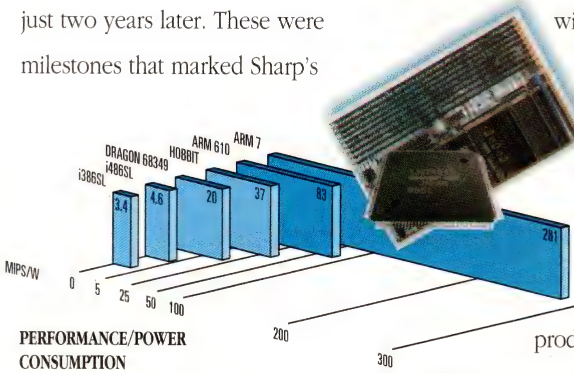

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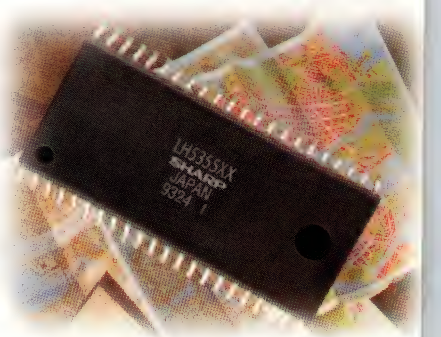

Sharp's newest 8 Mb and 16 Mb MROM achieve their 50 ns access speeds by using a page-mode function that reads a page of information at once. Sharp offers an industry-leading 6 - 8 week turnaround time.

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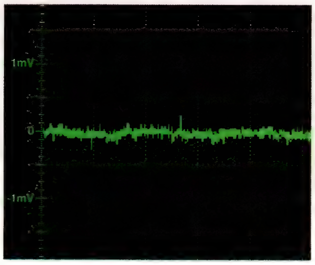

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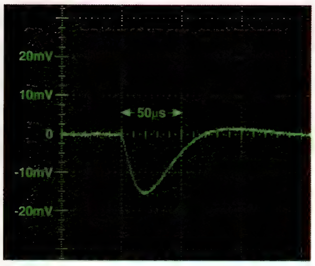

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READER SERVICE 97

POWERFUL "SOFT" COMPUTING TECHNOLOGIES EMERGE FROM THE FUSION OF NEURAL NETWORKS AND FUZZY LOGIC

In technology and science, the most exciting advances often come at the interfaces—the borderlines where two or more disciplines meet, greet, and cross over the neighboring fences. A fusion between two emerging technologies, neural networks and fuzzy logic, is creating a new hybrid technology area of "soft" computing that has significant potential for the future, according to leading neural-network researcher Dr. A.J. Maren, senior scientist at the Accurate Automation Co., Chattanooga, Tenn.

Maren notes that in the past two years, signs of this fusion have been quite clear. Both the World Congress on Neural Networks (WCNN), held in San Diego, Calif., this past June, and the IEEE International Conference on Neural Networks (ICNN), held in Orlando, Fla., also this past June, have had major sessions devoted to the neural-fuzzy linkage.

Books on these matters have gone through quite a transformation. It was only several years ago that literature on neural networks or fuzzy logic began to proliferate. Now, there's a significant body of literature that addresses both areas and the synergies that evolve by combining them *(see "For further reading," right)*. Among researchers, the most interesting applications seem to involve hybrid neural-fuzzy technologies. These have been applied to the tasks of pattern recognition, fault detection, image progressing, and control.

Two papers, each presented at the WCNN, illustrate how both fuzzy logic and neural networks can be applied to the same area—image processing/understanding—in very different ways. However, both approaches exploit one of the key differences between neural-network and fuzzy-logic methods: Neural networks excel at processing low-level, "signal" data, and fuzzy logic gives clues for using high-level, "symbolic" information.

In the WCNN Proceedings, W.T. Woo describes how a combined neural and fuzzy system was used to perform the two jobs of edge detection and image enhancement. A neural front-end was used to enhance a noisy image and find rough edges, while a "fuzzy associative memory" was employed to refine the edges and construct smooth edge boundaries. The advantage of his approach is improved computational cost when compared with certain adaptive filters, which perform better than either simple high-pass or low-pass filters on image processing.

In the same Proceedings, A.D. Kulkarni and others describe a "neural-network-based fuzzy-logic decision system," which they apply to multi-spectral-image classification. Fuzzy and neural capabilities are combined more intimately than was done in the preceding work.

Their system uses a neural-network-type architecture consisting of six "neural" layers. The processing is feedforward: the information in one layer feeds directly into the next, and so on. The network's first three layers are for "fuzzification"; the input values are mapped to membership functions that are used for fuzzy decision making. The last three layers implement fuzzy inference rules. They found that by incorporating fuzzy rules, they could substantially reduce the training time needed to teach the neural network.

Neural networks and fuzzy logic share similarities, but also have significant differences. Both areas have been around for a while. Neural networks has had a longer incubation phase (first work was done in the 1940s, and much significant work was done by many researchers in the 1970s), while fuzzy logic began with ground-breaking work by Lotfi Zadeh in 1965.

Both emerged as strong technologies in the late 1980s, when the limitations of traditional artificial-intelligence (AI) methods were becoming painfully apparent. They exemplify what can be called "numerical model-free estimators," and are dynamic systems. And each is a significant constituent of what has come to be called "soft computing", a set of computational methods that tolerate imprecision, uncertainty, and partial truth.

Neural networks consist of a set of individual simple processing elements, or "artificial neurons." Each neuron typically receives inputs (usually from other neurons), combines these inputs, applies a nonlinear

FOR FURTHER READING

For those unfamiliar with the subject, the July issue of *Computer Design* magazine includes a special report on fuzzy/neural fusion technology and design practices. Written by Tom Williams, "New tools make fuzzy/neural more than an academic amusement" provides practical insights on the state of the art and highlights some of the current design tools available. For those interested in pursuing the neural/fuzzy connection further, there are several excellent books available. An important book is Bart Kosko's *Neural Networks and Fuzzy Systems* (Prentice Hall, 1992). Another interesting and useful perspective is provided by *Computational Intelligence Imitating Life*, published by IEEE Press. This is an edited collection of invited articles from the first annual World Conference on Computational Intelligence. It provides an excellent overview of some important areas being addressed by fuzzy/neural fusion. Finally, for those not familiar with neural-network technology, the *Handbook for Neural Computing Applications*, by Dr. A. J. Maren et al., (Academic Press, 1990) is a good primer on this emerging field. It provides the reader with a solid base on the theory of neural-network technology and considerations for practical applications.

transfer function, and passes the result on to other neurons. The connections between neurons are called "connection weights," and much of the effort in developing a good neural network goes into "training" these weights to take on useful values.

Training is done by presenting the neural network with samples of inputs, observing the difference between observed and desired outputs, and changing the connection weights until the observed outputs approach the desired outputs. The output is typically a classification of the input into one of several categories, or an enhancement or completion of the input (as in the case of the image-processing example discussed earlier).

Neural networks often are used to handle time series as well as static data, producing very good results. Once a neural network is trained, it can typically produce good results even with noisy or incomplete data.

Fuzzy logic began with fuzzy set theory, developed by Lotfi Zadeh. The concept of fuzzy sets—or of fuzziness in general—offers a new way of looking at uncertainty.

Whereas previous probabilistic thinking dealt with the issue of randomness, uncertainty (for example, the degree to which some specific event takes on certain attributes or falls within a certain class) is different. It deals with ambiguity. As Bart Kosko, a leading fuzzy-neural researcher, describes it, "Whether an event occurs is 'random', to what degree it occurs is fuzzy."

Fuzzy set theory has led to fuzzy logic and fuzzy inference, which comes in the form of fuzzy associative mappings. Like traditional AI methods, fuzzy-logic methods are typically applied to high-level structured or linguistic data. Unlike traditional AI methods, fuzzy inferencing allows "rules" to be used with degrees of certainty, and conclusions to be drawn with differing degrees of certainty.

What's the implication of all these "soft computing" processes? Is it simply a way to get better loading for washing machines, self-focusing on cameras, and/or improving other small niches in the consumer electronics market? Maren speculates that "while these products capture immediate attention—and garner monies for more advanced R&D—the long-term goal of researchers in these areas is nothing less than true machine intelligence." As Lofti Zadeh, the father of fuzzy logic, put it, "In the final analysis, it may be argued that it is soft computing, rather than the traditional hard computing, that should be viewed as the foundation for AI. In the years ahead, this may well become a widely held position."

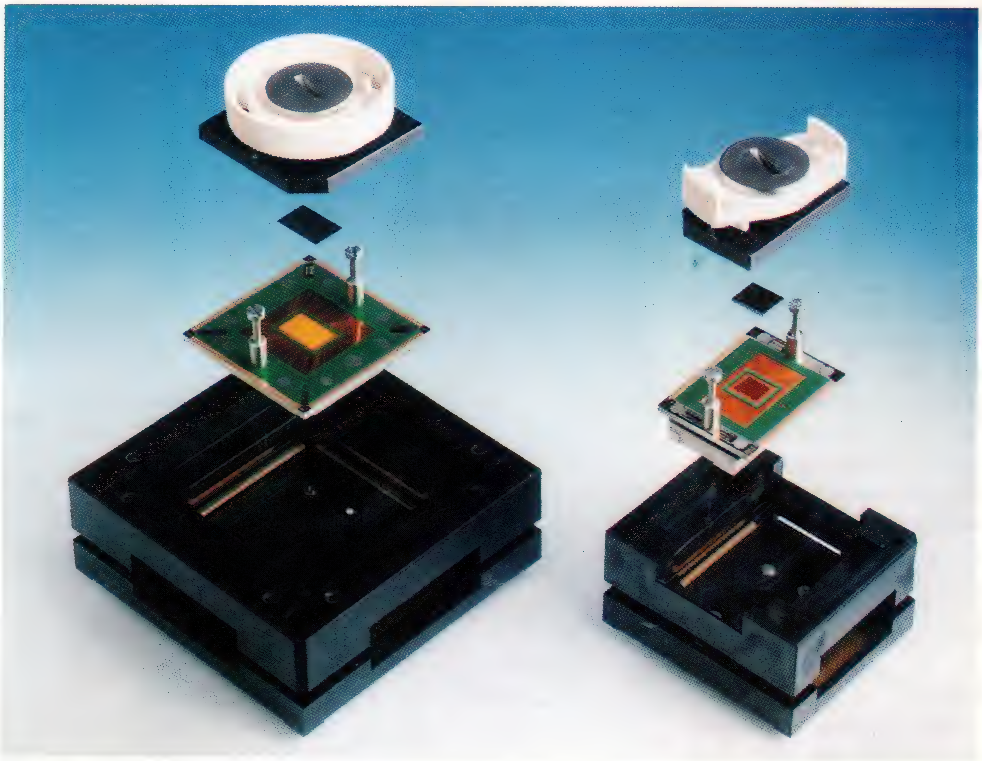
For further information on neural networks and their applications, contact Dr. Alianna Maren at P.O. Box 24714, Chattanooga, TN 37422 (615) 843-3751.

LEE GOLDBERG

PRODUCTION SYSTEM FACILITATES BARE-DIE TEST AND BURN-IN

A newly developed practical means of testing and burning in bare die just may be the ticket for screening known-good die (KGD) for multichip modules (MCMs) and hybrids. The economical system, which lends itself to either manual or automated operation, doesn't degrade die pads and performs electrical tests, burn-in, baking, at-speed testing, and other screening operations.

The system was created jointly by Texas Instruments' Metallurgical Materials Div., Attleboro, Mass., and MicroModule Systems (MMS), Cupertino, Calif. Called DieMate, it can perform functional IC tests at temperatures up to 15°C and speeds up to 250 MHz. It handles thermal cycling from –55 to +150°C and burn-in to +150°C. An initial endorsement was received from Intel Corp., Santa Clara, which is using the scheme for test and burn-in of its SmartDie bare-die products (ELECTRONIC DESIGN, *July 11, p. 44)*.



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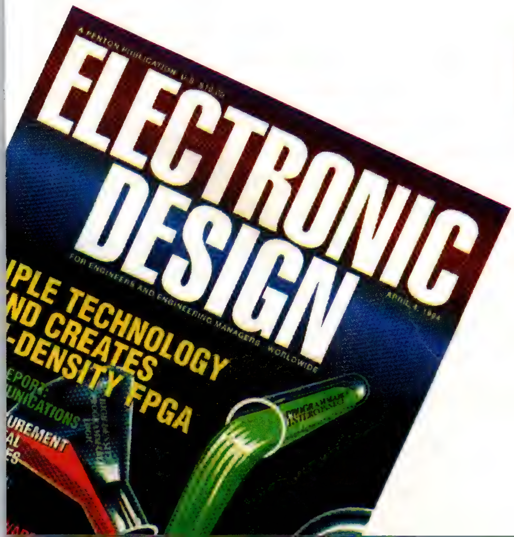

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Seven supplements released yearly focus extensively on specific topics. Supplements make great reference sources for electronic design professionals.

Two parts make up the DieMate system *(see the photo)*. One is a reusable die carrier that acts as a temporary IC package for die testing and handling. The user simply loads an IC die face-down onto the carrier manually or with pick-and-place equipment and then attaches the lid. The second part is a test and burn-in socket capable of high-speed functional testing and a full range of temperature screening. The loaded carrier drops into the open-top design of the socket after pressing down on the socket cover. Such a design permits the use of standardized burn-in boards.

Although the DieMate carrier and socket can be employed manually, they're designed for automated use. The top and bottom of the reusable carrier can be inserted into sockets, test handlers, or carrier trays by pick-and-place equipment. The socket requires minimal actuation force to open its contacts, allowing the carrier to be dropped into place.

The carrier's base assembly includes a thin-film copper/polyimide membrane fabricated by MMS. The membrane contacts the bond pads on the die with a series of gold-plated bumps coinciding with bond-pad coordinates. These bumps are topped with a proprietary oxide-penetrating feature that provides a non-wiping contact interface with the die. In this way, the system makes temporary contact with the bond pads without degrading them.

Signal traces are routed to the carrier's edge, where contact pads connect to the socket. The membrane bumps also are compliant and will adjust to any mechanical dissimilarities between the die and the substrate.

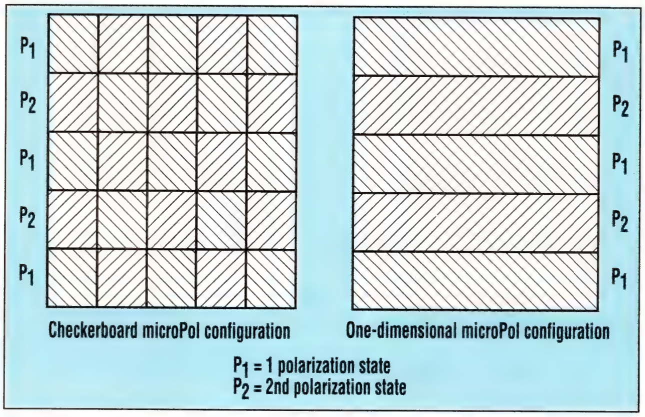
Rigorous alpha-site testing indicates that the reusable die carrier is capable of 500 cycles. The high cycle life is a key factor in keeping test costs for individual die low. TI estimates that per-die costs can be as little as $0.25 to $0.50, depending on volume and process-flow rates. DieMate systems with 56-, 110-, and 280-pin sizes are in production, and a 400-pin version is in the planning stage.

For more information on the DieMate system, contact TI at (508) 699-3800.

DAVID MALINIAK

OPTICAL ELEMENT COMBINED WITH LCD TECHNOLOGY ENABLES 3D DISPLAY CAPABILITY

A polarizing optical element known as a microPol has made it possible to produce three-dimensional stereoscopic active-matrix liquid-crystal displays (AMLCDs) that surpass conventional 2D systems and other 3D technologies in the areas of quality, flexibility, and cost. In fact, because people have stereo vision, an AMLCD device equipped with a microPol element can produce stereo images that will enhance the processing as well as the visualization of information in various applications.


P1
P2
P1
P2
P1
Checkerboard microPol configuration
P1
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P1
P2
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One-dimensional microPol configuration
P1 = 1 polarization state
P2 = 2nd polarization state

The process used to produce these 3D stereoscopic AMLCD devices, microPol optical technology, is based on an array of small polarizers oriented in alternating polarization states during the display process. As a result, a true sense of depth is given to computer-generated images.

Today's 3D display technologies have actually dominated a number of technical industries for some time. Though these devices enable the viewing of 3D images, they typically require slides and transparencies, as well as bulky, costly headgear. In addition, conventional devices are plagued by the problems of image flickering and ghosting. In situations where reliable, high-quality images and compact portable equipment are the defining characteristics, conventional display devices simply don't make the grade.

Reveo Inc., Hawthorne, N.Y., in an attempt to address these issues, came up with the microPol optical technology that can produce the stereoscopic depth perception required for viewing 3D images. Fabricated using advanced microfabrication techniques, the microPol element combined with today's advanced display technology produces AMLCDs with greatly increased resolution and realistic depth. As a result, typical microPol-enhanced display products are more powerful, reliable, and cost-effective than current 3D systems.

The microPol optical element is made up of a periodic array of microscopically small polarizers that spatially alternate between one polarization state, or direction, and another polarization state perpendicular to the first. The size of each micropolarizer can be as small as 10 µm. As a result, a microPol element could have more than 100,000 micropolarizers of alternating polarization states. Depending on the desired effect, the polarizers can be configured into one of two possible configurations, either a checkerboard arrangment or a one-dimensional configuration *(see the figure)*.

The process of stereoscopic imaging and viewing requires the presentation of two views of an object, both the left and right perspective, for a viewer's left and right eye, respectively. When these two perspective views are combined, a composite image that contains both the left- and right-eye information is formed as a result. By alternating this image on a line-by-line basis, a spatially multiplexed image (SMI) is created.

When combining these two technologies in a pro-

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DM2212	1Mb x 4	15ns	7ns/35ns	300 mil SOJ
DM1M32, 36	1Mb x 32,36	15ns	7ns/35ns	72 pin SIMM
DM2M32, 36	2Mb x 32,36	15ns	7ns/35ns	72 pin SIMM

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jection system or display, the microPol element component is responsible for the task of polarization encoding of the left and right image lines of the SMI during the display process. In this process, a microPol element of the same spatial period as the SMI is placed over the SMI, so that the alternating left-eye and right-eye information lines have alternating polarizations.

Upon viewing through an appropriately oriented polarizer rotated by 90 degrees, a person's left eye observes the left view and that viewer's right eye observes the right view. Subsequently, the human brain fuses the two images, producing stereoscopic depth perception. This demultiplexing operation enables both the left and right eyes to collectively view a composite stereoscopic 3D image through passive polarizing glasses.

One prime implementation of microPol optical technology is the VR-1000 stereo projection panel manufactured by VRex, a subsidiary of Reveo. This high-performance, portable multimedia tool provides realistic depth perception. It achieves this by projecting computer-generated 3D stills, animation, and viewing images.

Using a thin-film-transistor (TFT) color AMLCD, the VR-1000 stereo projection panel features a high-resolution microPol element, a pixel resolution of 640 by 480, a contrast ratio of 100:1, and an active display area of 7.5 by 5.7 in. Yet it's quite light , weighing in at only 5.5 lbs.

The 3D images projected from the AMLCD screen may be viewed using inexpensive passive glasses, eliminating the need for costly, bulky electronic headgear. With its high resolution and unique 3D capabilities, all due to the implementation of microPol optical technology, it stands out as one of the industry's first computer-generated 3D image-projection system.

It's conceivable to foresee the implementation of microPol technology in numerous other applications. One such application, CyberBook, a 3D stereoscopic notebook computer, would allow cost-effective stereoscopic presentations to be viewed anytime, anywhere on an AMLCD screen with the use of passive glasses.

Future implementations of microPol optical technology may find its place in any one of a number of applications for various industries. These applications include CAD/CAM, CAE, communications, training, robotics, scientific visualization, space, and simulation. They also include multimedia and virtual reality.

Both the VR-1000 stereo projection panel and the CyberBook stereoscopic notebook computer are currently available for purchase. Additional technical information and cost details may be obtained by contacting either Reveo Inc. at (914) 345-9555 or its subsidiary VRex Inc. at (914) 345-8877.

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MULTIBANKED ARCHITECTURE PROVIDES FAST, FLEXIBLE, AND REDUNDANT DRAMS

Today's designers of DRAM-based memory subsystems for graphics and other high-performance applications have an arsenal of memory options to choose from. However, most available high-performance choices—generic video RAMs; Window RAMs available from Samsung Semiconductor Inc., San Jose, Calif.; generic synchronous DRAMs; cache DRAMs available from Mitsubishi Electronics Co. of America, Sunnyvale, Calif. and Ramtron Corp., Colorado Springs, Colo.; and the unique RDRAMs made by RAMbus, Mountain View, Calif.—carry with them some penalties.

One of those penalties is a larger chip area than a standard DRAM and, consequently, a higher price tag. In a few cases, memory access latency is the issue, rearing its head most when accesses must be done randomly throughout the memory space. Latency is less of an issue when long sequential strings of data are transferred.

Now, a novel DRAM architecture that combines an array of small, independent DRAMs on one chip not only provides very fast read and write access times, but also gives users degrees of flexibility and redundancy that were previously unavailable. Furthermore, the forthcoming memory will address all three key factors—high performance, competitive pricing with DRAMs, and simple system implementation.

Developed by MoSys Inc., San Jose, Calif., the multibank DRAM, known as an MDRAM, integrates an array of "N" independent DRAMs, each 256 kbits, onto a single semiconductor chip.

Each MDRAM bank is organized as 256 rows and 128-byte columns. The novel MDRAM device is also quite fast. Its Read and Write times starting with the Column Address Strobe signal are just 15 ns and 6 ns, respectively.

Data is transferred in bursts to or from the MDRAM—the first word input to the memory is a starting address, which activates one of the N DRAM banks and specifies the location of the first data word to be accessed. Bursts of up to 128 bytes can be clocked in or out using both the rising and falling clock edges (two transfers per clock cycle) before the address must be changed.

The short initial access times and the burst-transfer capability give the memory chip a wide bandwidth of more than 660 Mbytes/s over its 16-bit-wide data bus when operating at its top clock rate of 167 MHz. In contrast, the Rambus RDRAM offers a top transfer rate of 500 Mbytes/s but

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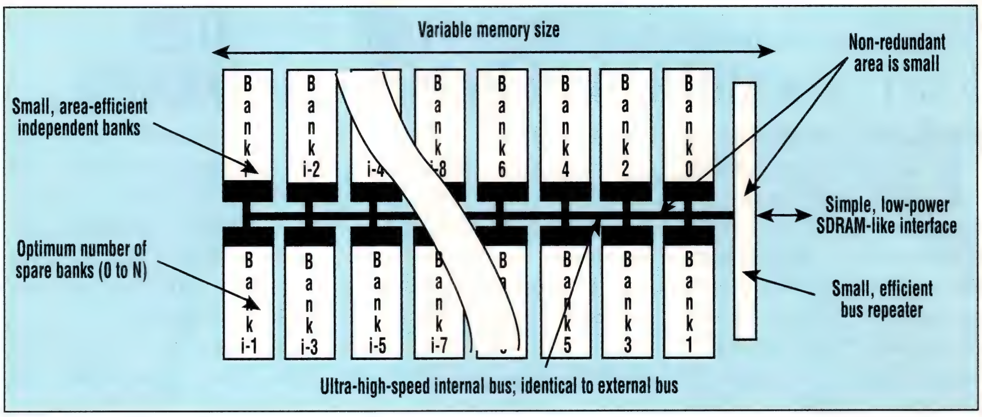
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Simple, low-power SDRAM-like interface
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Bank i-4
Bank i-8
Bank 6
Bank 4
Bank 2
Bank 0
Bank i-1
Bank i-3
Bank i-5
Bank i-7
Bank 5
Bank 3
Bank 1

must be clocked at a frequency of 250 MHz to achieve that throughput. Synchronous DRAMs operating at a frequency of 100 MHz deliver a peak throughput of several hundred megabytes/s over a 16-bit interface.

Each 256-kbit block is a complete DRAM, fabricated using 16-Mbit memory design rules, ensuring that the small blocks are very fast. Moreover, because the blocks only have to drive an on-chip metal bus, they can be accessed very quickly.

All of the blocks have a 16-bit data-bus interface and are tied to a central data and control bus. This 16-bit central data bus is connected to repeaters that buffer the signals and then feed them to the outside world over a 26-pin host interface, which operates in a manner similar to that of synchronous DRAMs *(see the figure)*.

The multiple banks also improve overall net bandwidth, especially in the case of small block transfers. They allow various operations to be time-multiplexed and minimize lost time due to latencies between transfers.

For example, a novel MDRAM clocked at a frequency of 75 MHz can provide faster transfer rates than high-speed single-port DRAMs for memory transfers of less than 64 bytes/request. In addition, when operated at a frequency of 100 MHz, the MDRAM provides a higher net bandwidth than any other memory approach for transfers of less than 128 bytes.

Each memory block includes its own address decoder, read/write control logic, and redundancy control elements. The central data bus that interconnects all blocks routes every signal to the host-computer interface. The interface includes small but high-efficiency bus repeaters that can drive the signals off the chip or distribute the incoming signals across the chip.

One unusual aspect of the architecture opted for by MoSys' designers is that all signals are routed off or onto the chip from a single edge of the chip. That allows for a simple interconnection scheme when multiple chips are connected together, and also minimizes the amount of chip area required for bonding pads. On top of that, the multiple-bank approach lowers overall chip power consumption: Because each bank has its own address decoder, the bank will only become active when it detects an address match. As a result, only one of the "N" banks on the chip will be active at any one time, which keeps power drain down to a minimum.

The architecture's high memory-area-to-logic-area ratio also reduces the amount of area required by non-redundant circuits. This in turn diminishes the chance that a manufacturing defect will totally disable chip operation by hitting one of the non-redundant sections. Furthermore, the high memory-to-logic ratio as well as the 16-Mbit DRAM process rules will yield a chip area that's comparable to standard DRAMs, which means that the chips also will be competitively priced.

During the manufacturing process, each memory block is assigned an address through a mask step. When the DRAMs in the array are tested prior to being packaged, bad blocks are disabled and good blocks are "reassigned" by disabling the default address and programming in (via laser-blown fuses) the new address. Thus, any bank can replace any other bank to repair defects. That means all chips free from non-redundant area defects can be sold.

In addition, just three days are needed to define a new mask set to implement MDRAMs with custom-defined capacities and granularity. The resultant memory could then be optimized for a specific capacity/cost point. To further reduce cost, the final memory still could use the same test program, leadframe, package, and pinout.

When the host-computer interface receives a starting address, all blocks will examine the incoming address and the matching block will activate. Unlike standard DRAMs in which row changes are slow and column changes are fast, the MDRAM, due to its banked architecture, has no long row latency time because the independent banks can be "cached" to minimize access delays.

Furthermore, unlike chips such as the Rambus RDRAM that has burst latency of 50 or more 2-ns clock edges, the MDRAM has a single-bank decoding delay of just 15 ns to reach the first data word. The 16-bit-wide architecture, when combined with the flexibility to quickly define any memory depth, lets designers create chips optimized to match the system granularity. In contrast, using standard catalog parts (such as 1-Mbit or 4-Mbit memories) in graphics subsystems often results in some unused memory, because the DRAMs have too much capacity for some screen resolution/color combinations.

Samples of the first multibank DRAMs will be released in the late third quarter. In addition, MoSys has contracted with three DRAM foundries and lined up several alternate-source partners who will also sell the high-performance MDRAMs.

For further information on the novel MDRAM, contact Gary Banta at (408) 321-0770.

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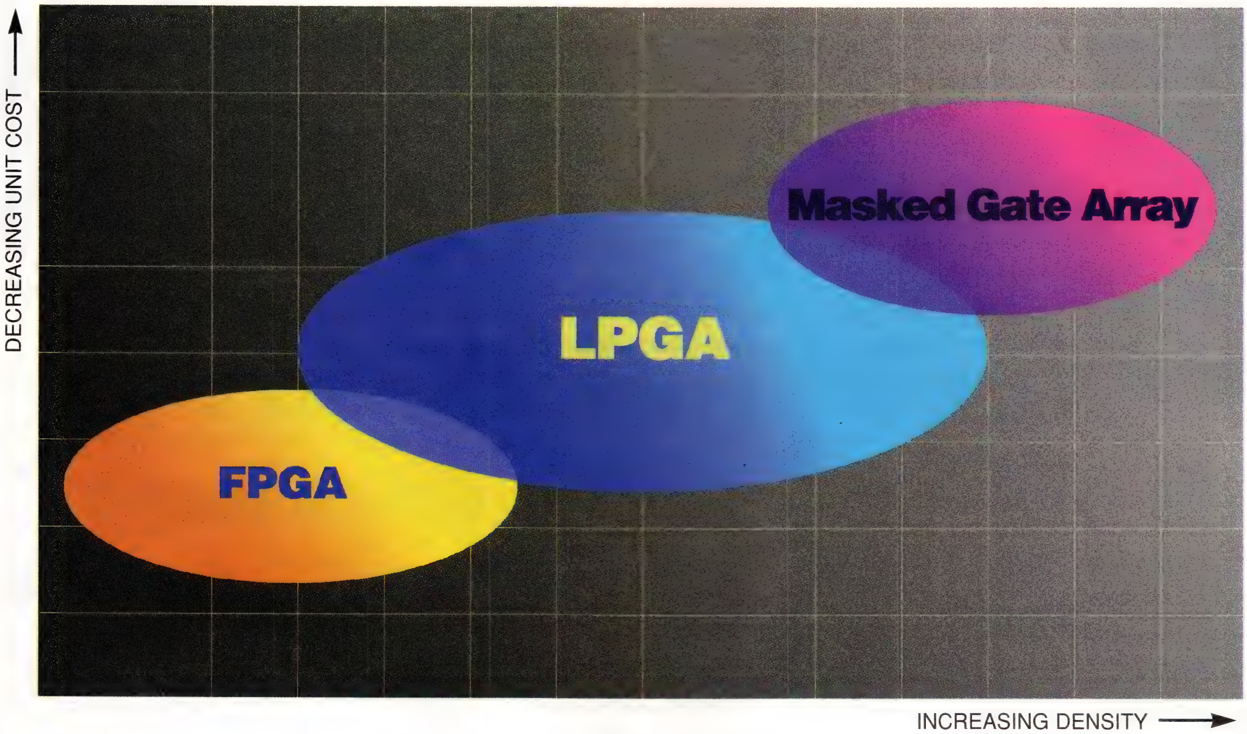

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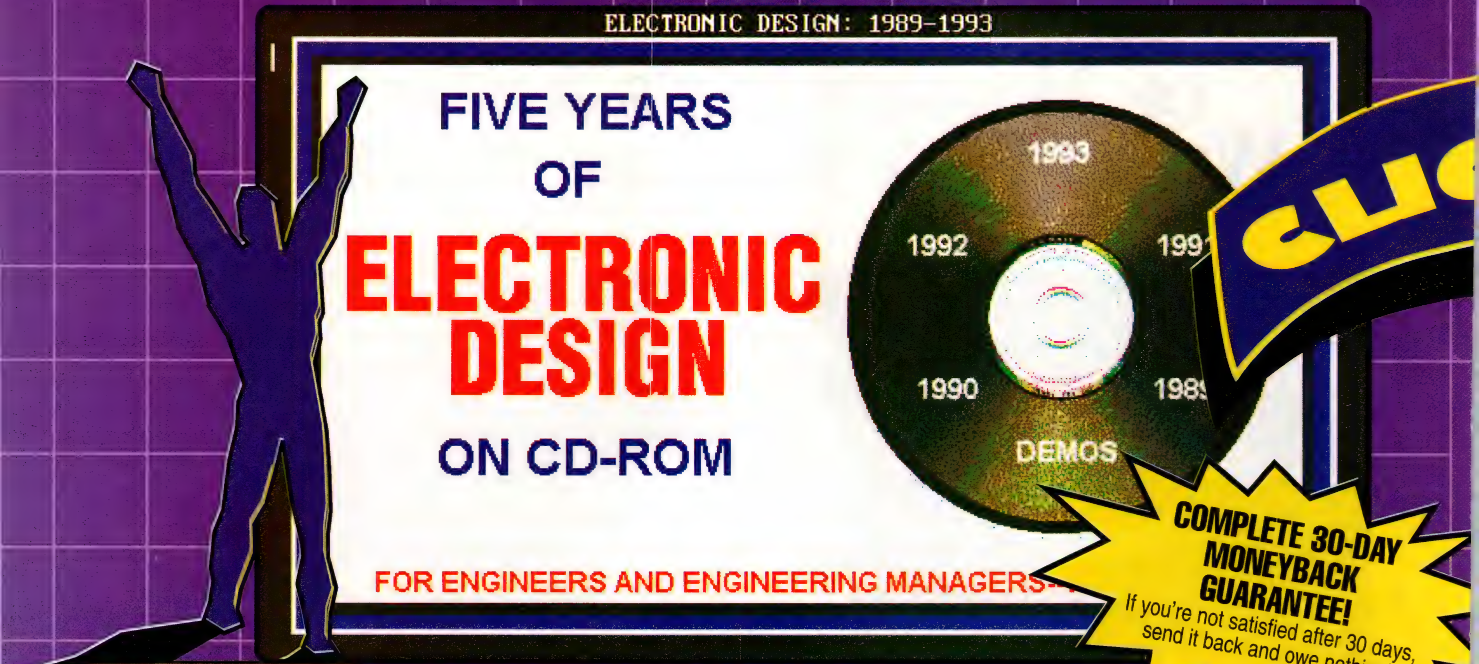
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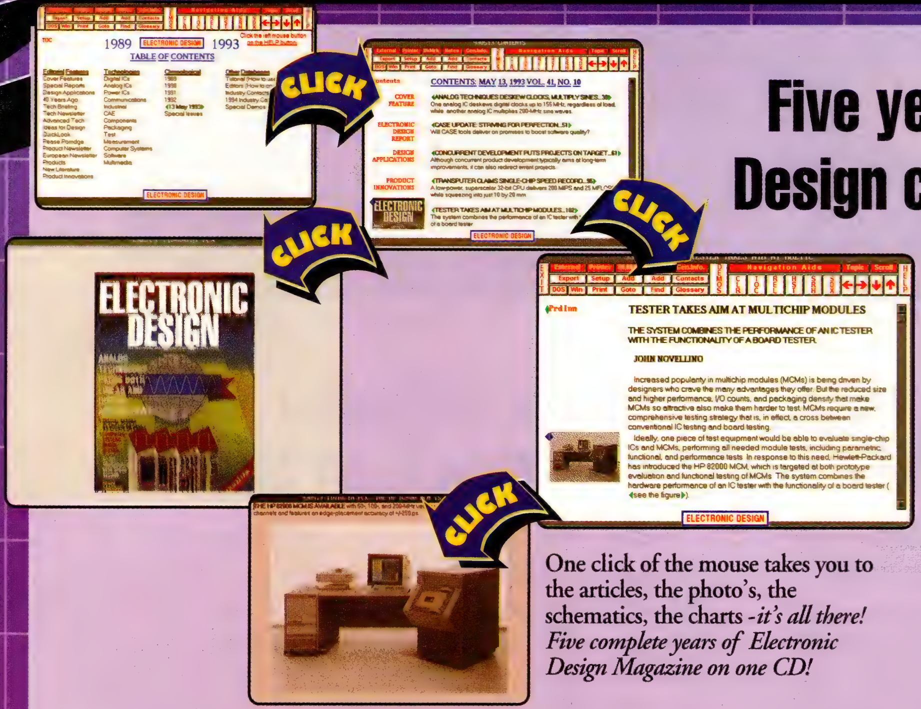

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TESTER TAKES AIM AT MULTICHIP MODULES

THE SYSTEM COMBINES THE PERFORMANCE OF AN IC TESTER WITH THE FUNCTIONALITY OF A BOARD TESTER.

JOHN NOVELLINO

Increased popularity in multichip modules (MCMs) is being driven by designers who crave the many advantages they offer. But the reduced size and higher performance, I/O counts, and packaging density that make MCMs so attractive also make them harder to test. MCMs require a new, comprehensive testing strategy that is, in effect, a cross between conventional IC testing and board testing.

Ideally, one piece of test equipment would be able to evaluate single-chip ICs and MCMs, performing all needed module tests, including parametric, functional, and performance tests. In response to this need, Hewlett-Packard has introduced the HP 82000 MCM, which is targeted at both prototype evaluation and functional testing of MCMs. The system combines the hardware performance of an IC tester with the functionality of a board tester (see the figure).

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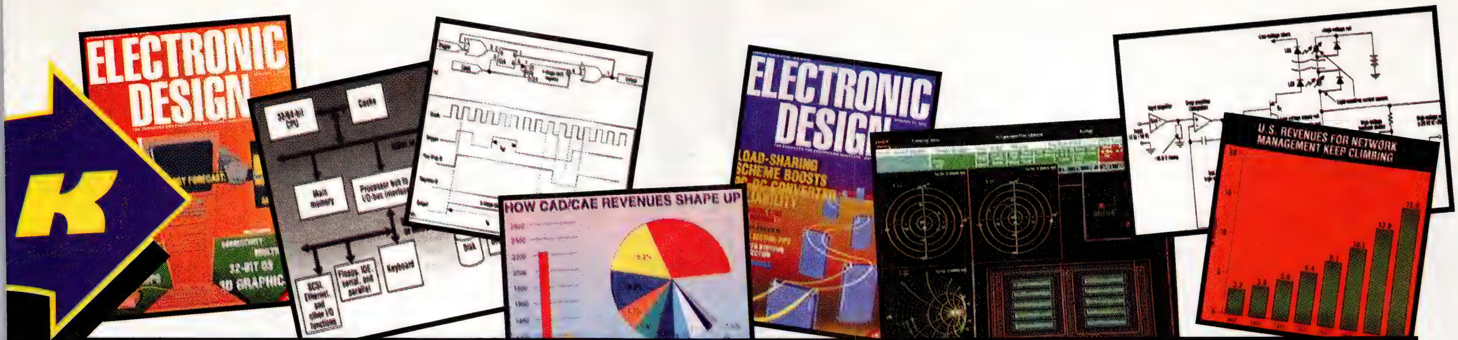
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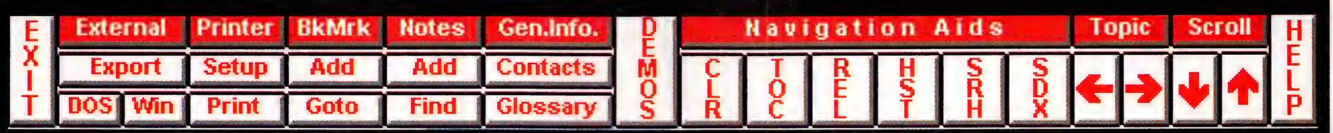

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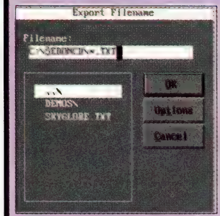

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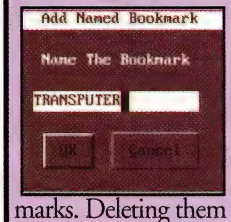

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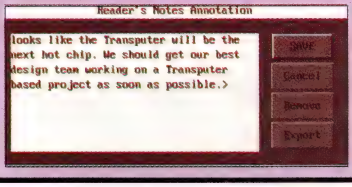

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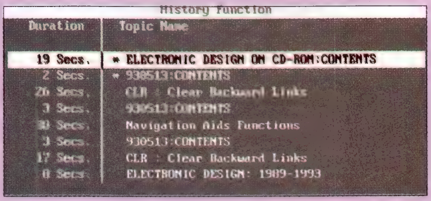

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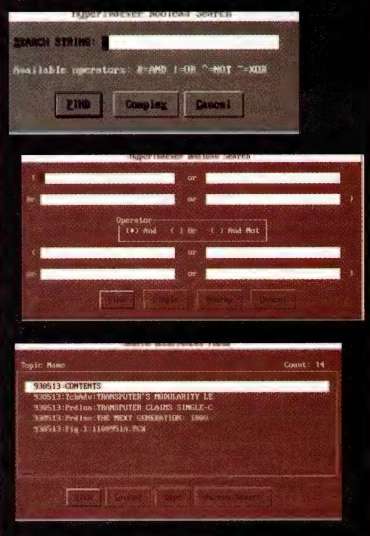

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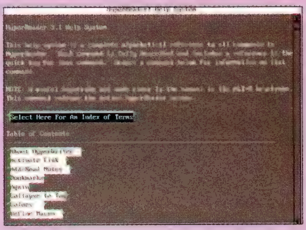

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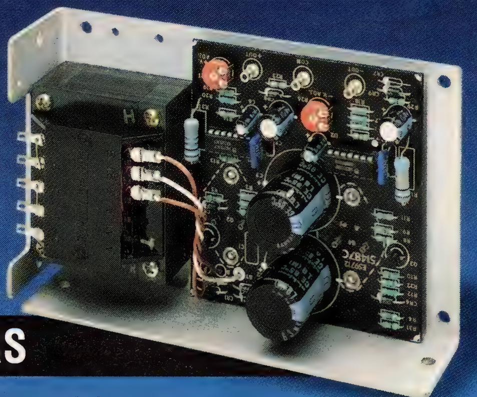

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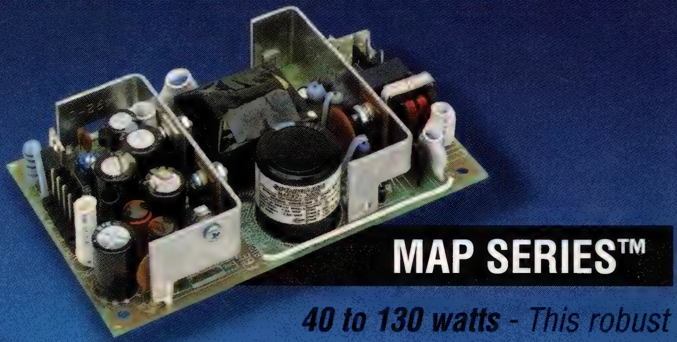

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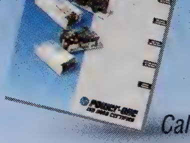

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READER SERVICE 124

HIGH-SPEED MODEMS: THEY'RE NOT JUST FOR DATA ANYMORE

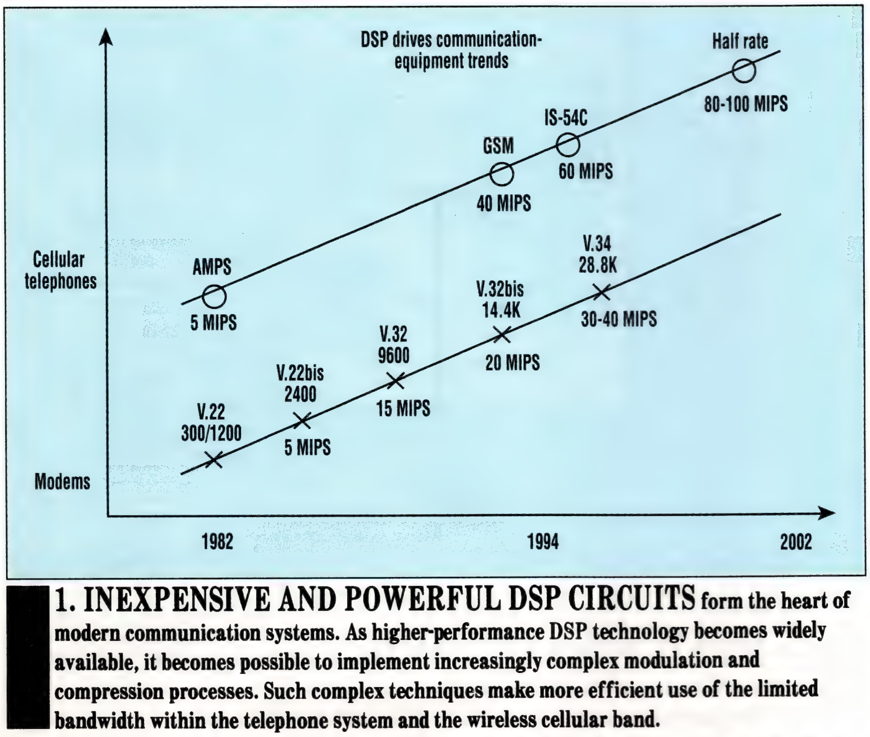
INNOVATIVE MODEM TECHNOLOGIES PUMP DATA, FAX, AND VOICE-MAIL AT BLAZING SPEEDS. JUST HOW DO THEY GET THOSE 114 KBITS ON THAT 3-KHZ LINE?

LEE GOLDBERG

High-speed modems are essential for survival in a world that thrives on fast, easily accessible data. There's an almost bottomless demand for products offering higher transmission rates which reduce both waiting time and telephone connect charges for large file transfers. Over the past few years, technologies have evolved that help data-hungry users squeeze increasingly fast data streams into the narrow 3-kHz pipeline originally meant to transmit grainy sounding voice signals. Rapid advances in technology coupled with high consumer demand has ensured that designers have a wide range of high-speed modem chip sets to choose from *(see the table)*.

The most recent development in this quest for speed is the finalization of the V.34 protocol, which can support communication at up to 28.8 kbits/s. With additional compression techniques, some systems are able to achieve effective throughputs eclipsing 100 kbits/s over standard telephone lines *(see "V.34: A closer look," p. 50)*.

More than just an evolution of current protocols, V.34 represents a quantum leap in complexity, requiring significantly more processing power to support it *(Fig. 1)*. The new, higher data rates also have some interesting side benefits. Along with handling increasingly sophisticated data protocols, today's modem chip sets use their powerful signal-processing capabilities in multiple roles to provide other functions, such as fax, voice-mail, and low-speed video. In addition, several techniques have been developed to split the modem's bit stream into two channels, allowing for simultaneous transmission of voice and data.



1. INEXPENSIVE AND POWERFUL DSP CIRCUITS form the heart of modern communication systems. As higher-performance DSP technology becomes widely available, it becomes possible to implement increasingly complex modulation and compression processes. Such complex techniques make more efficient use of the limited bandwidth within the telephone system and the wireless cellular band.

Though the ink on the V.34 protocol isn't even dry, a number of modem manufacturers have already released their first implementation of the version of V.34 that will be submitted for final approval early this fall. Other vendors are still selling parts that use the pre-release version of V.34 (dubbed V.FAST by the industry) and will soon issue new V.34-compliant software to clear up the minor discrepancies between the two protocols. This is possible because of programmable digital-signal-processor (DSP) technology used in most (but not all) high-speed modem chips.

Even the previous generation of V.32-based protocols were very complex and evolved rapidly into higher performance variants of the original standard. To cope with this, most manufacturers turned to high-performance, general-purpose, programmable DSPs rather than redesign dedicated logic every time a faster modem standard was introduced. In such a device, the executable code is stored in an external ROM or downloadable RAM to permit easy upgrading as standards evolve.

Designers working with these faster, more intelligent, V.32 and V.34 devices will find that modems have transformed from being fairly straightforward VLSI components to complex communications subsystems, often with their own embedded software and book-like data sheets. On a positive note, much of the required analog interface circuitry has been placed on a single chip or replaced with DSP filter functions, reducing parts count and pc-board area requirements. Similarly, most or all of the "glue" logic and host-computer-system interface circuitry is incorporated into the modem chip sets themselves. In addition, these chips are usually designed to be downward-compatible with virtually every previous modem and fax standard that's been widely used over the past 20 years.

Before we begin examining the modem chip sets themselves, let's take a quick look at the evolution of the last few generations of modem protocols. Still somewhat popular among low-end computer users is V.22-compatible modems. The original V.22 protocol specified that data be moved at a lumbering 1200-bit/s rate. Its improved variant, the V.22bis standard, delivers 2400 bits/s, which is adequate for many simple tasks. Chips adhering to these two protocols have been on the market long enough to slide far down on the price curve, making them good candidates for applications where cost is the overriding concern.

Currently, most modems being produced employ the V.32 family of protocols, which start at 9600 bits/s. The first extension to this protocol is the V.32bis standard. V.32bis takes advantage of some of the unused bits in the V.32 startup sequence, making it possible to add an enhanced mode that boosts the transmission rate to 14.4 kbits/s. The V.32terbo modulation is a simple extension of its predecessor, V.32bis, which uses the last two available startup sequence bits to enable an enhanced coding scheme that supports data rates to 19.2 kbits/s.

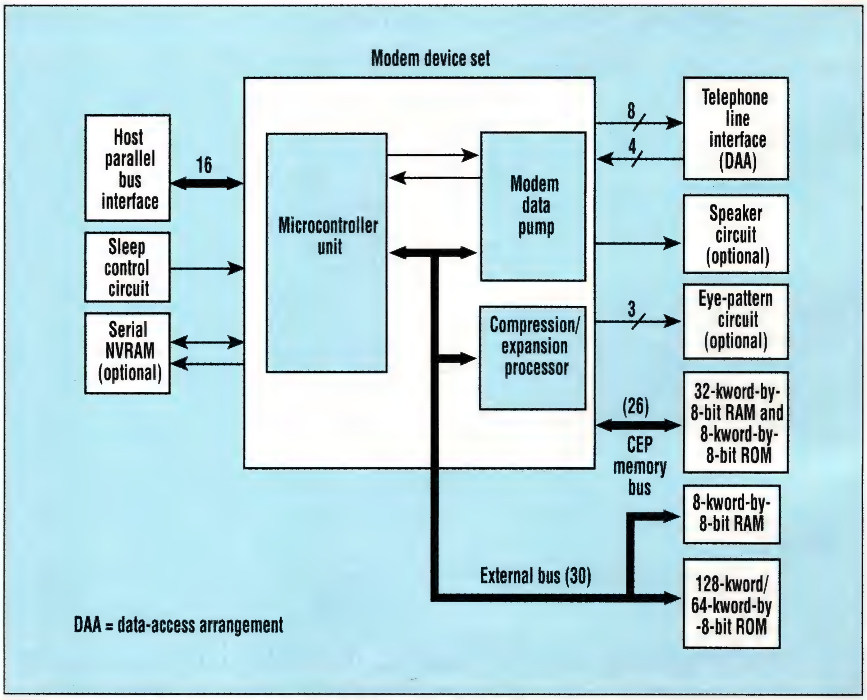
While not as fast as V.34, these V.32-class products offer very good cost/performance ratios because component prices are dropping as the market matures. Moreover, the simpler V.32 controllers require much less code and computational power than their V.34 counterparts.

Because fax transmissions employ a technology similar to that used in data modems, many manufacturers offer their chips with fax capability. Most modem-chip vendors support at least the V.29 protocol, which delivers a 9.6-kbit/s data rate. Many offer a V.17 mode at 14.4 kbits/s. In fact, at least one chip maker (AT&T) has already rolled out a device that supports V.17terbo data at 19.2 kbits/s.

A modem can be described as a collection of several functions. Each manufacturer makes architectural decisions on how to implement each function and which functions to group within a particular chip. These decisions directly affect the performance, flexibility, and cost of the chip or chip set being produced.

MODEM ARCHITECTURE

The actual modem function is usually referred to as a data pump, a device that translates digital information into the properly modulated waveform for transmission and performs the inverse function for incoming data. Some data pumps employ a specialized array of dedicated analog and digital logic circuits to perform this task while others use a general-purpose DSP circuit and


Modem device set
Host parallel bus interface
16
Sleep control circuit
Serial NVRAM (optional)
Microcontroller unit
Modem data pump
Compression/ expansion processor
8
4
Telephone line interface (DAA)
Speaker circuit (optional)
3
Eye-pattern circuit (optional)
(26)
CEP memory bus
32-kword-by-8-bit RAM and 8-kword-by-8-bit ROM
8-kword-by-8-bit RAM
External bus (30)
128-kword/ 64-kword-by -8-bit ROM
DAA = data-access arrangement

2. A TYPICAL MODEM ARCHITECTURE using dedicated logic is illustrated in this block diagram. This system uses Rockwell's RC288ACi series chip set. Note the outboard compression/expansion processor, which increases performance.

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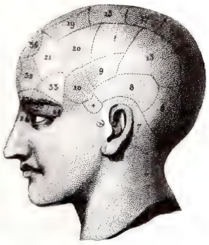

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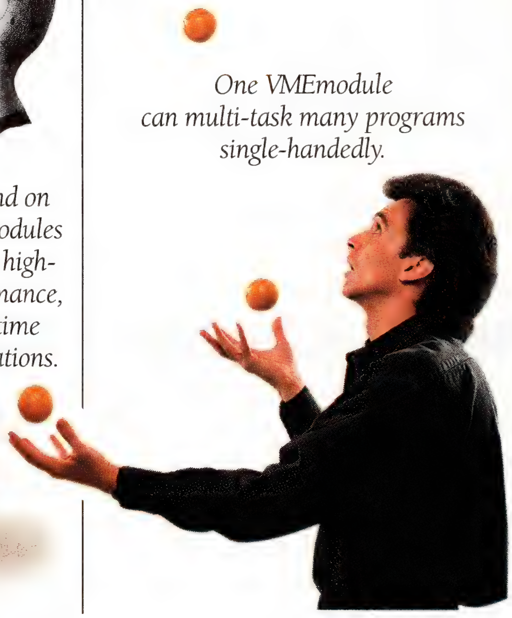

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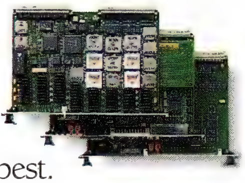

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specialized code. If a DSP-style data pump is chosen, a codec function is required to translate between the digital format of the processor and the analog line signal. A separate line-interface function performs signal conditioning, isolation, and impedance matching between the data pump and the telephone line.

A controller function orchestrates the overall operation of the modem, providing directions to the data pump and controlling the flow of data to and from the host-computer system. The controller usually performs error control, data compression, communication with the host-computer system, and line-control functions. In addition, the controller is usually responsible for implementing a command set that permits the host-computer system to control the modem. Most often, the Hayes modem "AT" command set is used as a de facto standard.

The host interface function serves as a data and command path between the modem and whatever system it's connected to. For external or stand-alone applications, a serial interface is typically chosen.

Ordinarily, a parallel interface is used to tie the device directly to the

V.34: A CLOSER LOOK

After two years of intense debate, the recent unanimous approval of V.34 by the ITU study group has modem vendors racing to develop compliant 28.8-kbit/s products. To understand why the V.34 effort took so long, and why designing compliant modems is so difficult, you have to understand the scope of the standard and how it differs philosophically and technically from other standards.

For modem makers, V.34 presents two problems. First, its faster signaling rates and more robust encoding schemes require faster DSP ICs. Second, its unprecedented level of flexibility requires a much more complex modem design.

The new standard is defined with a maximum signaling rate of 28.8 kbits/s operating over the general switched telephone network and over two-wire leased lines. In addition, V.34 should be able to run at slower speeds in 2400-bit/s increments (26.4 kbits/s, 24 kbits/s, and so on) if required due to adverse line conditions.

A fundamental difference between V.34 and previous standards is that V.34 allows connection-time configuration of almost all modem transmission parameters. Although differences exist between say V.22 and V.32 modem families, each standard is based on a single set of fixed parameters that include symbol rate, a data-encoding scheme, transmission power, and others.

V.34, on the other hand, implements a complex setup scheme where these parameters are negotiated at the start of each call and set according to the highest common denominator of the two modems' capabilities and the transmission characteristics of the telephone line in use. For example, both modems will be able to choose from various carrier frequencies, permitting each modem's signal to be shifted in frequency enough to fit into the channel's available passband at any V.34 symbol rate.

Just as in V.32, V.34 modems utilize quadrature-amplitude modulation (QAM), where symbols are modulated based on phase and amplitude. These phase and amplitude combinations mapped into real and imaginary space cause the 2D mapping of symbols into a "constellation."

Constellations contain the minimum number of points (distinct combinations of phase and amplitude) necessary to support a given data rate. They're arranged to yield the maximum distance between points. In V.32 constellations, there are 2^n symbols, where n is the number of bits per symbol. For instance, an uncoded 9600-bit/s constellation contains four bits per symbol and a total of 16 symbols. Receiving any one of these symbols would convey 4 bits of data.

When V.32 was being developed, engineers noted a high probability of normal Gaussian noise occasionally affecting either the phase or amplitude of the bit stream. This caused errors in the received data. However, trellis coding eliminated the problem of ambiguity in V.32 modems.

Trellis coding basically establishes a limited set of valid point sequences. In other words, for any given point in the constellation, there are only a few other points that can be subsequently transmitted. Moreover, each of the possible subsequent points is represented by a significantly different amplitude-phase combination (not an adjacent point in the constellation). Because the receiving modem knows which points can be received next in the transmitted sequence, it can correctly interpret a "near miss." In effect, trellis coding yields the equivalent of a 3-dB improvement in immunity to Gaussian noise.

To encode data, V.34 depends on a trellis-coding scheme similar to the one developed for the V.32 mode. While the 2D 8-state trellis code used in V.32terbo can support V.34's higher symbol rates, noise immunity can be increased by using a more complex code. The V.34 specification uses codes based on 4D symbols (the equivalent of two 2D symbols) and actually defines a choice of three codes: a 4D 16-state Wei code, a 4D 32-state code, and a 4D 64-state Wei code.

None of the V.34 trellis codes offer an advantage in terms of the number of bits a symbol can represent. They only offer differences in terms of immunity to Gaussian noise traded off against the complexity of the decoder.

The combination of trellis codes and faster symbol rates directly affect the DSP horsepower required in a V.34 modem. For example, the decoder complexity of computer bus when the modem is mounted on the motherboard or on a bus card. Many manufacturers also offer PCMCIA-compatible host interfaces, either as part of the host-computer interface or as a single-chip add-on.

There are several ways to assemble these functions into chip-sized chunks, depending on the intended application and fabrication technology available to the IC manufacturer. Some companies like Rockwell International have chosen to implement their modem function as a dedicated circuit rather than a general-purpose DSP circuit, so that they can optimize performance and reduce chip size. In Rockwell's family of modems, the dedicated data pump is driven by a single-chip controller that can be supplied by the company or several other vendors, such as Intel, Motorola, or Zilog *(Fig. 2)*. An outboard compression/expansion processor may be added to the configuration for higher performance. This dedicated-hardware configuration offers the advantages of low cost, low parts count, and less external memory requirements to support the modem.

The disadvantage to such a dedi-

the 4D 16-state code is about equal to the complexity of a 2D 8-state V.32 decoder. But the 64-state decoding task is 16 times more complex. In total, V.34 requires around 35 to 40 MIPS of DSP processing power, whereas V.32 requires only 20 MIPS.

V.34 and V.32 symbols also differ significantly. For example, V.32 always has an integer number of bits/symbol (i.e. the number of constellation points is always a power of 2). When trellis coding is used, a bit/symbol coding overhead is needed. In a 14.4-kbit/s modem based on a symbol rate of 2400, for example, there are 6 data bits per symbol. An additional bit for coding results in a constellation of 2^7 or 128 points.

V.34 modems, however, must support a wide variety of symbol and bit rates—as many as 9 data bits/symbol are needed to support a 28.8-kbit/s data rate at 3200 baud. Many of the bit-rate/baud-rate combinations even require a non-integer number of bits/symbol, called fractional bit rates. For example, at a data rate of 26.4 kbits/s and a symbol rate of 3200, there are 8.25 bits/symbol.

Another V.34 innovation is the fact that only 1/2 a bit of trellis-coding overhead is necessary per symbol. Cutting coding overhead in half relative to V.32 lets V.34 reserve valuable bandwidth for more data.

To handle the I/O associated with fractional bit rates, V.34 specifies a series of frames to group symbols in such a way that the frames will represent an integer number of bits. V.34 actually defines four different frame structures:

- A 4D symbol (a pair of 2D symbols). Because 2D symbols require 1/2 bit of coding overhead, each 4D symbol then requires one full bit.
- A mapping frame consisting of four 4D symbols for use in a V.34 technique called shell mapping.
- A data frame that contains multiple mapping frames, each of which can vary by ±1 bit. In this way, a data frame contains an integer number of bits and can at the same time enable a low-speed secondary channel to be injected into the data path.
- A superframe that combines a sufficient number of data frames to realize a constant number of bits/frame, regardless of the symbol rate.

The V.34 specification also allows for variable power transmission. Furthermore, it defines a number of optional transmission techniques to ensure maximum data rates on any connection. These include:

- Adaptive preemphasis. This alters the transmitting modem's output to compensate for amplitude distortion across the frequency band, effectively minimizing the amount of work handled by the adaptive equalizer.
- Precoding, which also helps the adaptive equalizer. Precoding effectively whitens noise on the channel to minimize the high-frequency noise being boosted by the equalizer.
- Nonlinear coding. This increases immunity to nonlinear distortion due to quantizing noise in a digital network. It causes distances between constellation points to be non-equal. For instance, points in a region less susceptible to noise are closer together and further apart in more sensitive regions. A similar warping technique was previously used in V.32terbo modems.
- Shell mapping, which allows for constellation expansion or shaping. Shaping assigns a cost to regions of points based on their distance from the origin, and concentrates the most frequently used points near the center (lower power) on the trellis-code constellation. This means that average transmit power is minimized, thereby increasing noise immunity.

The V.34's plethora of symbol rates and options are a problem for the analog front end. Customarily, with a fixed set of communication parameters, a modem would use a linear circuit in the front end for filtering. In V.34 modems, however, the filter parameters must change on a connection-by-connection basis to match the chosen parameters.

One solution is to use the DSP IC and software to implement the traditionally linear circuits. The DSP circuit's horsepower can simply set filter parameters at connect time and optimize the font end for prevailing line condition and communication modes. This substantially reduces the required analog components and leads to a much more compact design—especially key for compact portable applications. For exam-

(continued on p. 52)

cated system is flexibility. If there's sufficient computing power to support it, a general-purpose, DSP-based modem system can be upgraded to follow the evolution of communication standards as well as add new features via software upgrades rather than a "forklift" solution. Many manufacturers now offer configurations that employ downloadable RAM to store their executable DSP and controller codes. This permits hardware-free upgrades to existing products and lets vendors use the host computer's disk drive or slower, less-expensive types of nonvolatile memory to store the modem's operating instructions.

Today, one of the most popular configurations employed in DSP-based architectures is an integrated controller/host-computer interface chip, a DSP chip, and an analog front-end chip *(Fig. 3)*. This division of functions allows designers flexibility in design and the freedom to choose a controller that's best suited to interface with the targeted host-computer system. Manufacturers such as Analog Devices, AT&T, Cirrus Logic, and Phylon have adopted variants of this approach. Texas Instruments also produces a segmented architecture that employs its TMS320C5x DSP IC and a specialized ASIC to provide the glue logic to integrate the controller, DSP, and interface functions.

As in most high-volume products,

V.34: A CLOSER LOOK

(continued from p. 51)

ple, the 50 MIPS offered by the AT&T's DSP1600 core affords enough cycles to implement the front-end filters.

Two design problems arise from V.34's flexibility, however. First, V.34 only defines the capabilities required in the transmitter. The receiver can implement a subset of the total capabilities and still be within the specification. Second, the two modems must negotiate to establish which parameters to use in the data mode.

A predefined startup sequence is the solution to these problems. When two V.34 modems connect initially, they perform a startup sequence to negotiate a set of data-transmission parameters—the data mode. The ITU study group defined the first phase of the V.34 startup sequence in a separate specification known as V.8. Although V.34 is its first application, V.8 is a universal automoding scheme used in specifications for other modems as well as for faxes or other telecommunication devices. The remaining three phases of the startup sequence are defined in V.34.

Phase 2 of the startup sequence specifies that the modems probe the channel from both ends initially, with each modem transmitting test signals spread at 150-Hz intervals over the telephone-line bandwidth. During probing, each receiver makes decisions on the parameter set that will be used in the data mode. But first, the receivers must determine the maximum symbol rate the connection will support, and the optimal center frequency at that symbol rate.

Once the symbol rate is established, the modems probe the channel for Gaussian noise and determine whether the 16-state code is sufficient for optimal transmission, or whether one of the more complex codes is required. Regardless of the code negotiated, the modems also must agree on the number of bits each symbol will represent, as well as which other optional parameters will be used.

Each modem's receiver then sends the chosen parameters for the connection to the transmitters. It's not required to use the same parameters. The connection can operate at different speeds and with different parameters in each direction.

While the startup sequence sounds simple enough, it only ensures an interoperability baseline. In fact, a significant obstacle exists to complete compliance and interoperability at maximum speed, particularly with early implementations. V.34, like most specifications, includes items open to different interpretations by different designers. Early on, modems from different manufacturers will likely have some interoperability problems. These problems will dissipate as the market for V.34 products matures, and leading products in the market become the de facto standard.

During this period of clarification, designers will be wise to develop modems based on a software-upgradable architecture to ensure minimum user compliance and interoperability problems. Among others, AT&T offers a chip set called V.flex, which allows a designer to start with an easily upgradable RAM/flash-based design and then move to a ROM-coded design after the standard crystallizes. An SRAM/flash-based modem can be upgraded by the user via a floppy disk or a modem connection to a bulletin-board service.

The other key to low-cost modems is a complete V.34 implementation in a minimum number of chips. Typically, only a handful of ICs is needed besides the DSP IC (which typically requires a companion digital interface IC). The DSP and interface ICs constitute a data pump. A microcontroller also is required to handle functions such as the Hayes-AT command set, DTMF detection and generation, and error-correction and data-compression protocols such as V.42 and V.42bis. Like the DSP IC, the microcontroller will require more power than most of the ones used in V.32 designs—especially to handle V.42 correction and compression on faster data streams. Most modems also will need some SRAM, and upgradable designs require additional SRAM as well as flash memory.

Contributed by Martin Rauchwerk, product marketing manager, AT&T Microelectronics, Berkeley Heights, N.J.

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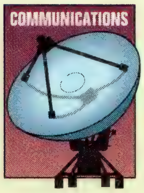

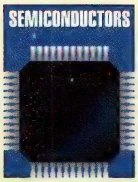

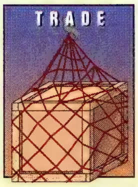

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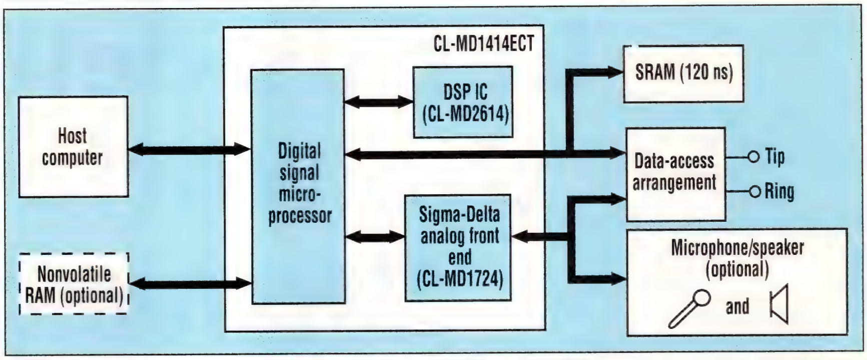
the trend toward increasing integration is now a fact of life for modems. AT&T's three-chip V.34 modem consists of an integrated controller/host-computer interface chip, a data-pump interface, and an integrated DSP/codec chip. TI also announced its intent to develop a two-chip solution in early 1995 and a single-chip modem with on-board memory by the end of next year.

Motorola's latest entry, the MC68356, is the closest thing to a single-chip solution available today. The chip manages to pack a DSP engine, a RISC controller, and a 68000-based microprocessor to handle interface functions on one chip, along with a PCMCIA interface and several kbytes of RAM and ROM *(Fig. 4)*. The only other components required for a complete system are some program memory for the interface controller, a codec, and a data-access-arrangement (DAA) circuit to convert the DSP IC's output to telephone-company-compatible signals.

While desirable for most applications, a single-chip approach isn't always the answer. These highly integrated chips are usually fairly expensive and might contain functions that can be provided by the existing host-computer system. If sufficient processing power is available, the CPU in a computer, game system, or cellular telephone may be able to perform the command-set implementation, compression functions, and other duties handled by a controller.

Another issue faced by chip manufacturers is where to put the computing horsepower required to perform the various functions. For the most part, the data pump is left alone to perform the complex modulation functions while the controller and host-computer interface worry about data compression, error control, and implementing a user command set. This typically requires a fairly powerful controller chip running at full speed to keep up with the V.32/V.34 data rates and associated functions.

Another approach was taken by Phylon with its PHY20XX series. The chip set's DSP circuit has enough MIPS power to handle its normal tasks as well as data compression and error control. This offloads the controller function sufficiently to permit the use of a low-cost, low-power controller chip, such as the Intel 8032.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Sigma-Delta analog front end (CL-MD1724)
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SRAM (120 ns)
Data-access arrangement
Tip
Ring
Microphone/speaker (optional)
and

3. THIS REPRESENTATIVE 3-CHIP MODEM, which employs DSP-based technology, is used in conjunction with Cirrus Logic's CL-MD1414ECT data/fax/voice chip set. The controller and host-computer interface functions are combined, with separate DSP and delta-sigma analog front-end chips.

A JUNGLE OF OPTIONS

The world of high-speed telephony isn't the place for the faint-hearted or acronym-phobic. Besides the actual V.32/V.34 protocols, there's an enormous pool of functions associated with these data rates that are designed to augment transmission speed, control transmission errors, and help the modems cope with "less than optimal" line conditions. Let's take a quick tour of this sometimes bewildering group of specifications.

Compression for V.22 through V.34 modems is usually handled by run-length encoding schemes. This means that the algorithm can "condense" the material being transmitted by picking out frequently occurring long bit patterns and replacing them with shorter codes. Because the data may be of any type, the scheme must be "lossless" to prevent corruption of software and data files. While many sound and image files can easily tolerate a few bits missing here and there, software and data files get downright mean when you knock out even a small chunk of their code.

One of the most successful early implementers of such a scheme was Microcom Corp., Norwood, Mass., a pioneer in the modem business. Prior to official codification of modem protocols by the International Telecommunication Union (ITU) and the International Consultative Committee on Telegraphy and Telephony (CCITT), many Microcom algorithms (referred to as MNP-x) were adopted as de facto standards by the industry. While recently superseded by the V.42bis compression scheme, many modems still carry the MNP-5 protocol so that they can be compatible with a large portion of the installed base.

Now that many modems have speech-processing capability, they can perform all kinds of new functions like voice-mail controllers or answering machines, which are discussed later in this article. The problem soon arises, though, when we realize that speech is pretty bulky stuff (128 kbits/s) in its raw form and will quickly eat us out of disk and RAM storage space if we try to store it in uncompressed form.

Most modems that handle speech have several compression schemes available to them. The simplest are a pair of algorithms called μ-law and A-law compression, which take 16-bit samples and turn them into 8-bit scalers, yielding a compression ratio of 2:1. Adding the Groupe Speciale Mobile (GSM) compression scheme used in European cellular telephones gives us an additional 5:1 squeeze for a more manageable data rate of about 13 kbits/s. Other compression schemes, such as the code-excited linear-predictive (CELP) algorithm, yield bit rates as low as 6.8 kbits/s while retaining good speech quality. Besides saving storage space, compressed speech is critical to efficient voice-over-data applications that share the modem's extremely finite bandwidth between a voice channel and data stream.

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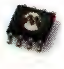

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You should also remember that any communication link is susceptible to errors and that noisy phone lines often are no exception.

ERROR CONTROL

Once again, the MNP 2-4 algorithms served as de facto standards until V.42 arrived on the scene. Many modems still support the MNP error-control standards, which can be invoked by non-V.42 modems as part of the call-setup procedure.

As an example, MNP-4 provides a modem with a handshake system, which allows retransmission of packets if they get lost or scrambled. This is very important when line quality is degraded by intermittent noise, caused by crosstalk, lightning, or other environmental factors.

Another clever trick employed by some modem chips is called "V.42bis over MNP-4," where the data is run through both the V.42bis compressor and MNP-4 error correction to squeeze the data close to its theoretical limit while adding another layer of error control. While such a trick can only be used when modems at both ends of the line support it, this will be handled automatically at the time the call is set up while data rates

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		Operating Modes													
		Data				Fax									
Company	Product	V.32	V.32bis	V.32terbo	V.34	V.22ter	V.29	V.17	V.17terbo	16550 UART Emul.	Voice Storage / Voice Over Data Modes	Architecture	Features/ Comments	Packaging	Price
Analog Devices Inc. One Technology Way P.O. Box 9106 Norwood, MA 02062-9106 (617) 329-4700 Fax 326-8703	AD20msp511/512 Series DSP-Based Modem Chip Sets	Y	Y	N	N	O	O	O	N	N	Software required for voice storage modes. / No voice-over-data modes.	3-chip set with integrated host-interface/controller, AD20msp511/12 DSP, and MSP01 integrated codec/signal conditioner.	Programmable DSP permits custom software to be developed for speech synthesis and sound-card emulation. Fax capability option. Parts kit for complete modem including software available.	PGA through PQFP	Call
	ADSP 2171/2181 DSP Microcomputers	S	S	S	S	S	S	S	S	N	Software required for voice storage. / Software required for voice-over-data functions.	Both 2171 and 2181 are scalable Harvard architecture DSPs with on-chip program and data memory. 2171 has 2-k RAM and 8-k ROM of memory and 2-k data RAM. 2181 has large internal 16-k by 16 data RAM suited for complex V.34 moduation code and 16-k by 32 program RAM. Requires controller chip.	Third-party software from VoCal and others supports V.32, V.34, voice storage and compression, and fax functions.	PQFP	$30-$35 10K lots
AT&T Microelectronics Dept. AL-500404200 555 Union Blvd Allentown, PA 18103 (800) 372-2447 Fax (610) 778-4106	HSM144/192 Series Data/Fax/Voice Modem Chip Sets	Y	Y	O	N	Y	Y	O	N	Y	AT standard voice command set and 13.3 Kbit/s GSM speech compression options. / No voice-over-data modes.	4-chip set with ROM-driven controller, seperate data pump, ROM-coded DSP, and linear codec.	Available in 14.4-k, and 19.2-k data/fax, 14.4-k data/voice/fax, and 14.4-k data/fax/cell configurations. Low-power chip sets available. Cellular direct-connect and MNP-10 error-correction options, Hayes AutoSync option.	PLCC and SOJ (desktop), PQFP and SOJ (portable), TQFP and PQFP (PCMCIA)	$49-$59 10K lots
	V32Cell series Land/Cellular Data/Fax Modem Chip Sets	Y	Y	Y	N	Y	Y	Y	N	Y	No voice storage modes. / No voice-over-data modes.	5-chip set with ROM/RAM-driven controller, seperate data pump, ROM-coded DSP, linear codec and single-chip PCMCIA interface.	Low power. Direct connect with AT&T, NEC, Fujitsu, and OKI cellular phones. Standard ETC and optional MNP-10 functions provide support for impaired cellular connections. Direct PCMCIA connect option. Hayes AutoSync option.	PQFP and QFP (portable), TQFP and VQFP (PCMCIA)	$69 10K lots

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Furthermore, they offer all the right connections. In fact, Yamaha chips connect at higher rates where other fax modem ICs fall back.

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and protocols are being established.

If you're designing a product that's intended for use in cellular systems or long runs through areas with poor-quality telephone lines, you should strongly consider the small extra expense in selecting a modem chip that supports either the MNP-10 or the ETC (Enhanced Throughput Cellular) protocol developed by AT&T Paradyne, Largo, Fla. These bundles of techniques were created to help modems cope with the noisy, rapidly changing line conditions found on cellular service.

Because cellular telephones are often used in mobile applications, the signal strength may vary quickly as a telephone moves between base stations at highway speeds. The disturbances experienced during handoffs and passage through dead zones are only two of the problems that a modem must contend with while talking over a cellular connection.

MNP-10 software provides adaptive transmitting techniques such as dynamic packet sizing and on-the-fly data-rate adjustment to keep the bits flowing as the signal strength and noise floor changes. As conditions worsen, MNP-10 adjusts packet size downward. This increases transmis-

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		Data				Fax									
Company	Product	V.32	V.32bis	V.32terbo	V.34	V.22ter	V.29	V.17	V.17terbo	16550 UART Emul.	Voice Storage / Voice Over Data Modes	Architecture	Features/ Comments	Packaging	Price
AT&T Microelectronics (continued)	HSM288 DSP163x-based Land/Cellular Data/Fax/Voice Modem Chip Sets	Y	Y	Y	Y	Y	Y	Y	Y	Y	GSM answering-machine emulation option. / Voice-over-data-software in development.	3-chip set includes controller, data-pump interface and integrated DSP/codec data pump. Designer may choose internal ROM or external downloadable RAM configurations. A second, external codec required for voice/data operation. Programmable DSP sets line-interface filter parameters for added adaptability. Optional PCMCIA interface chip available.	Low power. Direct connect with AT&T, NEC, and OKI cellular phones. Standard ETC and optional MNP-10 functions provide support for impaired cellular connections. Optocoupled line interface. Direct PCMCIA connect option. Full duplex speakerphone emulation option. Hayes AutoSync option. Downloadable RAM configuration allows software updates for new functions. Programmable host interface configuration supports Motorola, Rockwell, multiplexed, and non-multiplexed buses. Compression using μ-law, and A-law voice-thru modes.	PQFP and QFP (portable), TQFP and VQFP (PCMCIA)	$79-$95 10K lots
Cirrus Logic 3100 West Warren Ave. Fremont, CA 94538 (510) 623-8300 Fax (510) 226-2240	CL-MD1414ECx Series Data/Fax/Voice Modem Chip Sets	Y	Y	N	N	Y	Y	Y	N	Y	AT standard voice command set. 3/4-bit ADPCM and A-law voice compression. Telephone and answering machine emulation. / No voice-over-data modes	3-chip set with controller, DSP, and analog line/audio interface.	PC-ISA bus and PCMCIA direct interface options. Voice/fax/data auto-recognition. Complete telephone and answering machine emulation with interface for external microphone/speaker.	PQFP, PCMCIA, VQFP	$39-$43 10K lots
	CL-MD1414BA Series Data/Fax/Voice/Sound Modem Chip Set	Y	Y	N	N	Y	Y	Y	N	Y	AT standard voice command set, 3/4-bit ADPCM and A-law voice compression. Telephone and answering machine emulation. / No voice-over-data modes.	3-chip set with controller, DSP, and analog line/audio interface.	DSP can be used for high-quality sound-card emulation. Host interface includes DMA controller for high-quality audio applications. Complete telephone and answering-machine emulation with interface for external microphone/speaker.	QFP and VQFP	$40 10K lots

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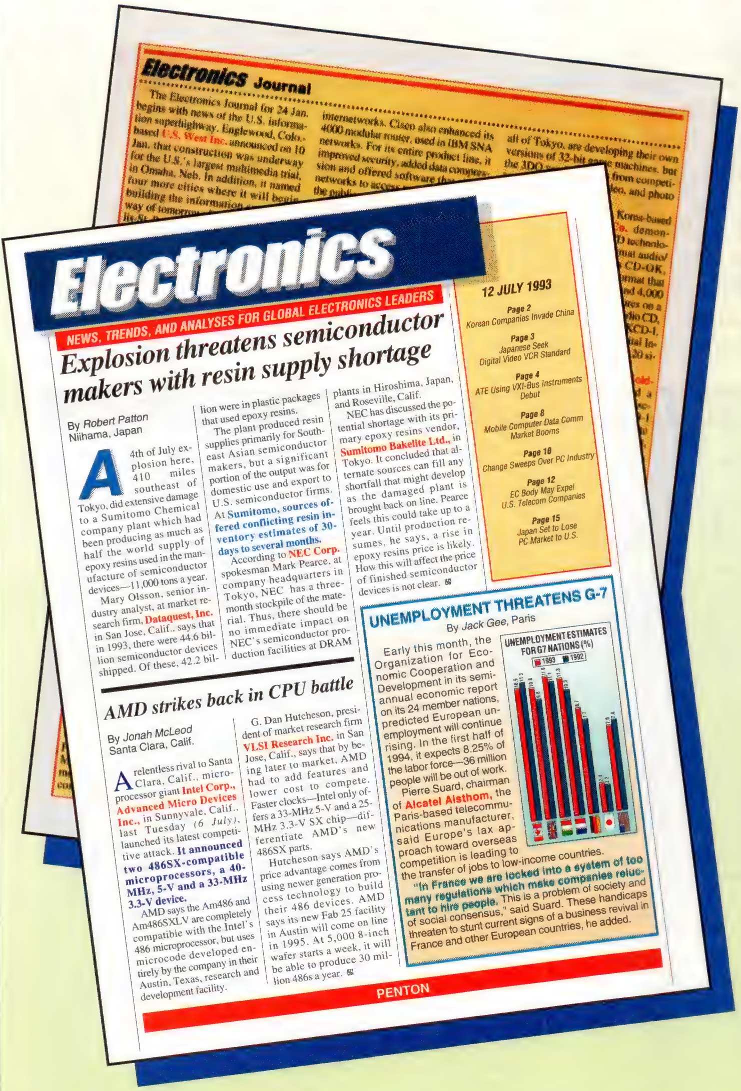

Electronics Journal

The Electronics Journal for 24 Jan. begins with news of the U.S. information superhighway. Englewood, Colo.-based U.S. West Inc. announced on 10 Jan. that construction was underway for the U.S.'s largest multimedia trial, in Omaha, Neb. In addition, it named four more cities where it will begin building the information

Electronics

NEWS, TRENDS, AND ANALYSES FOR GLOBAL ELECTRONICS LEADERS

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Japan Set to Lose PC Market to U.S.

Explosion threatens semiconductor makers with resin supply shortage

By Robert Patton
Niihama, Japan

A 4th of July explosion here, 410 miles southeast of Tokyo, did extensive damage to a Sumitomo Chemical company plant which had been producing as much as half the world supply of epoxy resins used in the manufacture of semiconductor devices—11,000 tons a year.

Mary Olsson, senior industry analyst, at market research firm, Dataquest, Inc. in San Jose, Calif., says that in 1993, there were 44.6 billion semiconductor devices shipped. Of these, 42.2 billion were in plastic packages that used epoxy resins.

The plant produced resin supplies primarily for Southeast Asian semiconductor makers, but a significant portion of the output was for domestic use and export to U.S. semiconductor firms. **At Sumitomo, sources offered conflicting resin inventory estimates of 30-days to several months.**

According to NEC Corp. spokesman Mark Pearce, at company headquarters in Tokyo, NEC has a three-month stockpile of the material. Thus, there should be no immediate impact on NEC's semiconductor production facilities at DRAM plants in Hiroshima, Japan, and Roseville, Calif.

NEC has discussed the potential shortage with its primary epoxy resins vendor, Sumitomo Bakelite Ltd., in Tokyo. It concluded that alternate sources can fill any shortfall that might develop as the damaged plant is brought back on line. Pearce feels this could take up to a year. Until production resumes, he says, a rise in epoxy resins price is likely. How this will affect the price of finished semiconductor devices is not clear.

AMD strikes back in CPU battle

By Jonah McLeod
Santa Clara, Calif.

A relentless rival to Santa Clara, Calif., microprocessor giant Intel Corp., Advanced Micro Devices Inc., in Sunnyvale, Calif., last Tuesday *(6 July)*, launched its latest competitive attack. **It announced two 486SX-compatible microprocessors, a 40-MHz, 5-V and a 33-MHz 3.3-V device.**

AMD says the Am486 and Am486SXLV are completely compatible with the Intel's 486 microprocessor, but uses microcode developed entirely by the company in their Austin, Texas, research and development facility.

G. Dan Hutcheson, president of market research firm VLSI Research Inc. in San Jose, Calif., says that by being later to market, AMD had to add features and lower cost to compete. Faster clocks—Intel only offers a 33-MHz 5-V and a 25-MHz 3.3-V SX chip—differentiate AMD's new 486SX parts.

Hutcheson says AMD's price advantage comes from using newer generation process technology to build their 486 devices. AMD says its new Fab 25 facility in Austin will come on line in 1995. At 5,000 8-inch wafer starts a week, it will be able to produce 30 million 486s a year.

UNEMPLOYMENT THREATENS G-7

By *Jack Gee*, Paris

Early this month, the Organization for Economic Cooperation and Development in its semi-annual economic report on its 24 member nations, predicted European unemployment will continue rising. In the first half of 1994, it expects 8.25% of the labor force—36 million people will be out of work.

Pierre Suard, chairman of Alcatel Alsthom, the Paris-based telecommunications manufacturer, said Europe's lax approach toward overseas competition is leading to the transfer of jobs to low-income countries.

"In France we are locked into a system of too many regulations which make companies reluctant to hire people. This is a problem of society and of social consensus," said Suard. These handicaps threaten to stunt current signs of a business revival in France and other European countries, he added.

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sion overhead but reduces noise-induced data loss by presenting a smaller target. The transmission rate also changes according to conditions, allowing the fastest rate possible at all times. While quite effective, MNP-10 requires that both the transmitter and receiver have MNP-10 functionality in order to use it.

The performance of AT&T Paradyne's ETC function compares favorably with MNP-10, but enjoys the advantage of being able to work if only one end of the transmission supports it. ETC also has a more sophisticated data-rate adjustment scheme that gives it a higher percentage of successful connections under harsh field conditions. Though not all of the features of MNP-10 or ETC can be used for land-line transmissions, they do provide an extra edge for maintaining the highest possible quality connection when calling areas with marginal telephone service.

HOST INTERFACES

There are several ways to get the data between the modem and its host. If the modem is to be located some distance from the host system, a serial interface is usually used to simplify the electrical connection.

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		Data				Fax									
Company	Product	V.32	V.32bis	V.32terbo	V.34	V.22ter	V.29	V.17	V.17terbo	16550 UART Emul.	Voice Storage / Voice Over Data Modes	Architecture	Features/ Comments	Packaging	Price
Cirrus Logic (continued)	CL-MD1414UN Series International Data/ Fax/Voice Modem Chip Sets	Y	Y	N	N	Y	Y	Y	N	Y	AT standard voice command set. 3/4-bit ADPCM and A-law voice compression, Telephone and answering-machine emulation. / No voice-over-data modes.	2-chip set with integrated controller/ analog line interface and DSP. External controller software in ROM or NVRAM supports international standards.	Manufacturer-supplied controller software available to support specific requirements for foreign markets. PCMCIA interface option. Complete telephone and answering-machine emulation with interface for external microphone/speaker.	SQFP and VQFP	$40-$42 10K lots Available 4th Q. 1994
Motorola Microprocessor & Memory Technologies 6501 William Cannon Drive West Austin, TX 78735-8598 Rex Kiang: (512) 891-2429	68356 Signal Processing Communications Engine	S	S	S	S	S	S	S	S	Y	Software required for voice storage and voice/data modes.	Enhanced single chip integration of a 68302-based communications and protocol controller, and a 56002 DSP with separate on-chip DSP program and data RAMs, controller data RAM, and a PCMCIA interface. Multiple DSP channels supported via a synchronous serial interface or external DSP parallel bus. Requires external codec and DAA for line interface.	On-chip PCMCIA interface. Low-power, 5-V and 3.3-V operation. On-chip memory eliminates external RAM from many applications. Manufacturer and third-party software available to support modem protocols to V.34 and fax protocols to V.17 plus AT command set, MNP-10 error correction and other functions. A variant chip called 68356M will be produced with on-chip V.34 modem firmware.	357p BGA	$64.95 10K lots Available 4th Q. 1994
Phylon Inc. 4027 Clipper Court Fremont, CA 94538 (510) 656-2606 Fax (510) 656-0902	PHY20xx Turnkey Data/Fax/Voice Modem Chip Sets	Y	Y	O	N	Y	Y	Y	N	N/A	ADPCM voice compression and storage. / No voice-over data function.	2-chip set with DSP and analog front-end. Provides all modem functions plus data/speech compression and error-control functions to reduce controller processing requirements. Simple, 8-bit external controller required, interfaces to modem via 8-bit bus.	Turnkey chip sets include licensed software for Intel 8032 controller. Also available without software. V.34-capable chip anticipated by end of 1994.	PLCC or TQFP	$38-$42 10K lots

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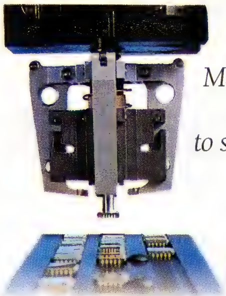

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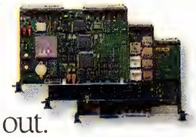

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		Data				Fax									
		V.32	V.32bis	V.32terbo	V.34	V.22ter	V.29	V.17	V.17terbo						
Phylon Inc. (continued)	PHY2111 Turnkey Simultaneous Voice and Data Modem With AT Controller	Y	Y	Y	N	Y	Y	Y	N	N/A	ADPCM voice-compression and storage. / Single-call TDM voice-over-data interlacing with dynamic bandwidth sharing.	2-chip set provides all modem functions plus data/speech compression and error-control functions to reduce controller processing requirements. Simple, 8-bit external controller required, interfaces to modem via 8-bit bus.	Turnkey chip sets include licensed software for Intel 8032 controller. AT command user-interface software provided in 'C' source code. V.34-capable chip anticipated by end of 1994. Can be interfaced to ISDN B-Channel.	PLCC or TQFP	$57-$63 10K lots
Rockwell Telecommunications 4311 Jamboree Rd. P.O. Box C Newport Beach, CA 92658-8902 (714) 833-4600	RC288Ci/VFC and RC244Ci/VFC Data/ Fax Modem Chip Sets	Y	Y	N	VFC	Y	Y	Y	Y	Y	No voice storage mode. / No voice-over-data mode.	2- or 3-chip set consisting of a controller, data pump, and optional compression/expansion processor. Serial and parallel user interfaces. NVRAM interface for parameter and table storage.	V.34 version anticipated soon. V.FC mode provides 28.8 kbit/s performance but is not fully V.34 compliant. World-class option supports multiple protocols, backlists, and filter parameters. Optional MNP-10 error correction for cellular and low-quality line applications. Hayes Auto-Sync option. Supports Hayes extended AT command set. Proprietary RC288/ 240DPi modem data pumps available separately for use with other OEM controllers.	PLCC	$72-$123 10K lots
Texas Instruments Inc. Literature Response Center P.O. Box 172228 Denver, CO 80217 (800) 477-8924, ext. 4500	TMS320C5x-based Modem Building Blocks	S	S	S	S	S	S	S	S	O	Software required for voice storage mode. / Software required for voice-over-data mode.	Building-block approach based around the TMS320C5x family of DSPs. Typical modem implementation requres DSP, controller, host interface, ASIC gate array, and line interface chips. Serial, bus-oriented (16550 emulation), or PCMCIA interface available.	Non-specialized architecture facilitates custom applications. DSP-based modem can be upgraded by software to meet evolving standards. 3.3-V and 5V operation. Customized DSPs and ROMs can be developed for high-volume applications.	TQFP	Call
Zilog Inc. 210 East Hacienda Ave. Campbell, CA 95008-6600 (408) 370-8000 Fax (408) 370-8056	Z80182 V.34 Modem Controller Chip	S	S	S	S	S	S	S	S	Y	Software required for voice storage mode. / N/A	Single-chip controller designed to drive standard data pumps (e.g. AT&T, Rockwell). Performs host interface, AT command set, data compression, error detect/correct, and flow control. Two DMA channels, serial and parallel host interfaces.	Third-party software available for applications through V.34 data and V.17 fax. Downloadable RAM architecture allows use of slow ROMs and permits easy software upgrades. Optional 86017 chip provides direct PCMCIA interface. 3.3-V and 5-V operation.	QFP or VQFP	$13.83 $14.36 10K lots

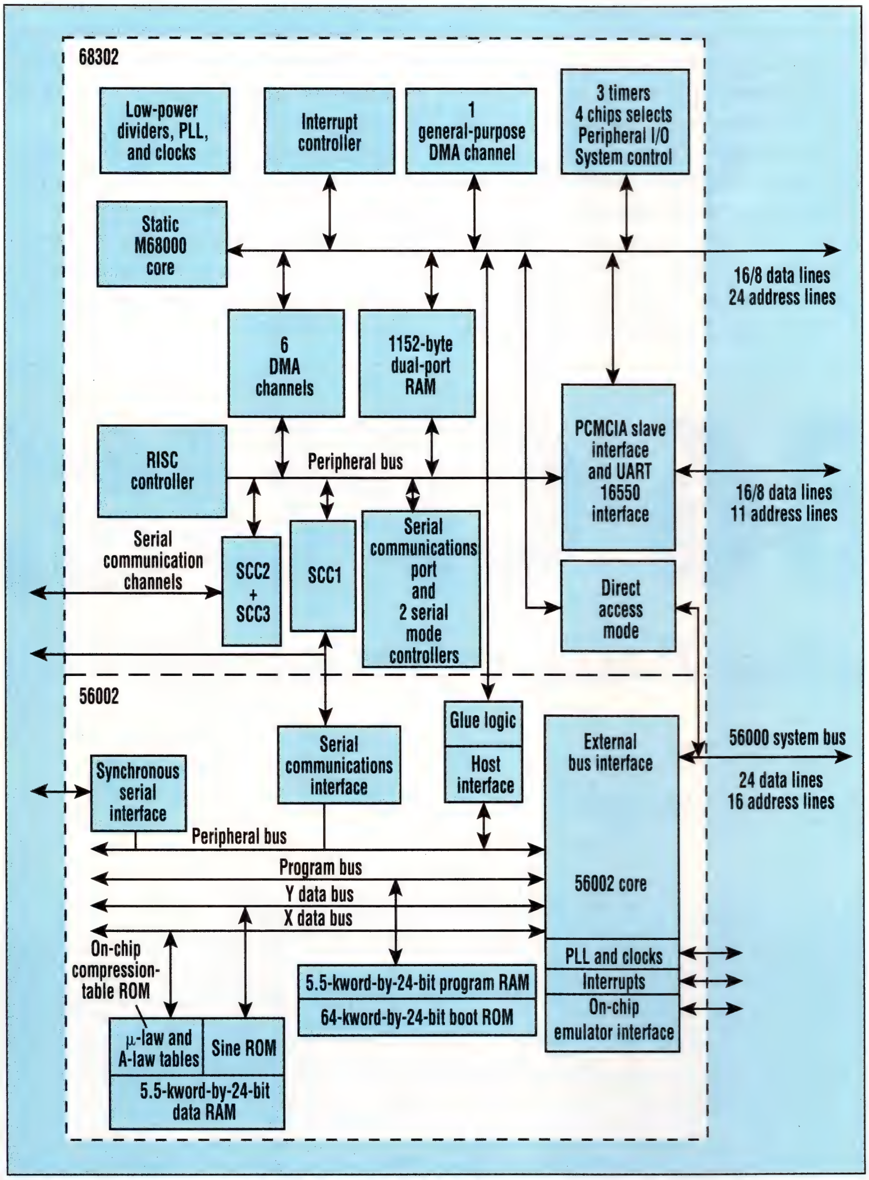
Y = Yes; N = No; O = Optional; S = Software-defined function; VFC = V.FastClass, a proprietary high-speed protocol developed by Rockwell that's similar but not identical to V.34.

Most chips support the RS-232 serial communication protocol, while others can handle more sophisticated formats like high-level data-link control (HDLC).

For bus-oriented systems, one of the most common ways to transport data is to make the modem's data and control interface emulate the parallel port of a 16550 modem chip. This provides a well-defined interface that almost any processor can use. If a modem has access to the host computer's data bus, it may use a DMA scheme to boost system throughput while lowering host-computer processing requirements.

For portable applications, PCMCIA is becoming the interface of choice because of its compact connector size and ability to interoperate with any other PCMCIA-capable device. Several manufacturers (such as AT&T and Cirrus Logic) offer chips with a built-in direct PCMCIA interface, but virtually any modem device can be interfaced using a low-cost PCMCIA bus adapter chip.

Two other functions will commonly show up on modem data sheets that can baffle the uninitiated. The "autobaud" feature is a standard part of V.32 and V.34 operation that allows two modems to negotiate a data rate based on their highest common speed and the condition of the telephone lines. Autobaud also supports rate renegotiation whereby the modems can adjust their speeds on-the-fly as line conditions improve or degrade.


68302
Low-power dividers, PLL, and clocks
Interrupt controller
1 general-purpose DMA channel
3 timers 4 chips selects Peripheral I/O System control
Static M68000 core
16/8 data lines 24 address lines
6 DMA channels
1152-byte dual-port RAM
PCMCIA slave interface and UART 16550 interface
RISC controller
Peripheral bus
16/8 data lines 11 address lines
Serial communication channels
SCC2 + SCC3
SCC1
Serial communications port and 2 serial mode controllers
Direct access mode
56002
Glue logic
Host interface
Serial communications interface
External bus interface
56000 system bus
24 data lines 16 address lines
Synchronous serial interface
Peripheral bus
Program bus
Y data bus
X data bus
56002 core
On-chip compression-table ROM
PLL and clocks
Interrupts
On-chip emulator interface
5.5-kword-by-24-bit program RAM
64-kword-by-24-bit boot ROM
μ-law and A-law tables
Sine ROM
5.5-kword-by-24-bit data RAM

4. THE COMPLEX ARCHITECTURE of the Motorola MC68356 signal-processing engine provides sufficient processing capability and I/O capacity to support all of the functions required for a high-speed modem on one chip. The DSP system-on-a-chip includes three processors, RAM, ROM, serial and parallel interfaces, several timers, and multiple DMA channels.

The Hayes Auto-sync function isn't part of the V.32/34 function, but it's offered as an option on many modem chip sets. When invoked, Auto-sync turns the normally asynchronous modem data stream into a synchronous link by adding synchronization protocol-control characters and filler bits to maintain a constant bit rate. This is particularly useful when communicating with mainframe-computer systems that are accustomed to talking with synchronous terminals. Since this is a proprietary communication algorithm, it will be licensed to the chip maker for a fee that's passed on as a nominal charge per chip for the option.

STANDARDS COMPLIANCE

When designing equipment for overseas markets, one must be compliant with the communications standards set by the telephone systems of the target country. These specifications usually involve the line impedances, signal levels, and signaling conventions that are unique to the country. Several countries attempt to protect their subscribers from harassment by limiting the number of times a device can attempt to dial a single number within a given period. This is known as "blackout" coding. While most modems will require a physical component change in their analog interface section to meet foreign impedance specifications, software-driven chip sets will be able to meet blackout and signal-level requirements with simple software changes.

Although much delayed, ISDN telephone services are beginning to become a real presence in some areas. Most likely, they will gain a strong foothold in the telecom market for businesses that are too large for a simple telephone system and too small for a T1/T3 subscriber service. Larger businesses also may benefit from ISDN's ability to perform complex call and service setup by using its signaling capabilities to communicate directly with the telephone company's switching system. Anticipating this, Phylon created a chip that's capable of communicating directly with an ISDN B-channel. Expect to see more companies offering this in the future.

VOICE/SOUND FUNCTIONS

Given the powerful processing capabilities available in today's modem chip sets, it's a shame to see all of that computing horsepower go to waste except when we want to go online. In addition to the previously mentioned fax functions, more and more manufacturers are using the DSP engines inside their chips to process voice signals for a wide variety of applications. The most obvious use of this capability is an answering-machine function, using either it's own memory or sharing the host system's RAM or disk for voice storage.

With a powerful, software-definable DSP system on the motherboard of a computer, the potential applications are only limited by the imagination of the designer. Using such voice-processing capabilities to create a high-quality speaker telephone function is another feature commonly found in many modem chip sets. At least one manufacturer (Cirrus Logic) even offers a version of its DSP-based data pump to emulate sound-card functions.

The computer's hard drive can store many minutes of compressed voice data in a single megabyte while operation and playback can be controlled from a "soft" panel presented on the display screen. Many vendors offer code that turns their chip into a GSM-standard answering machine as part of their controller and DSP software. Extra software can be added to allow remote control via touch tones. Further modifications would allow the same modem chip set to function as a voice-mail server for a small office.

The higher speed of today's modems offers the possibility of taking a portion of the bit stream and allocating it as a second channel for transmission of compressed digital voice data. Voice-over-data communications is still in its infancy, but the possibilities it offers are very exciting. A teleconference could employ a single line to carry voice at the same time that faxes were being passed between sites. Another scenario might involve a telephone conversation held between two engineers while data was passed between their computers and displayed on their screens as they talk.

If this catches on, who knows what the next generation of video games will look like? Perhaps people in different parts of the country will compete with each other in a common virtual landscape via conferenced modem hook-ups while they hurl

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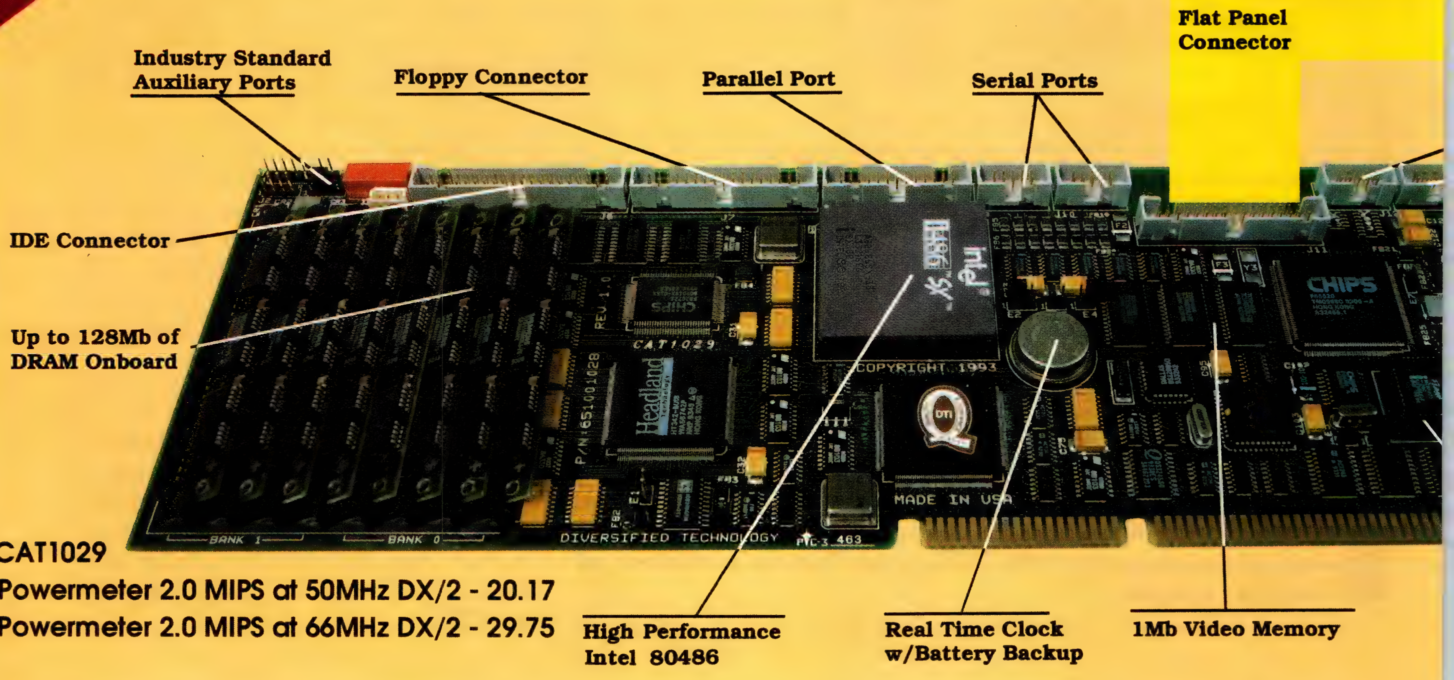
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1Mb Video Memory

CAT1029
Powermeter 2.0 MIPS at 50MHz DX/2 - 20.17
Powermeter 2.0 MIPS at 66MHz DX/2 - 29.75

threats and insults at each other.

Though a number of modem chip sets offer some version of simultaneous voice/data, no standard format exists at the moment. This means that both ends of a telephone line must have the same chip set attached to use the simultaneous voice/data function. The Telecommunication Industry Association's TR30.1 Committee is currently reviewing existing simultaneous voice/data technologies and is trying to develop recommendations for industry guidelines on the proper protocols.

One of the most promising simultaneous voice/data techniques on the market is the SingleCall protocol created by Phylon, Fremont, Calif., which is currently implemented in its PHY2111 modems. Phylon's approach is to digitize and compress the audio at the source and interlace the packets within the main bit stream using time-division multiplexing. Because voice contains long pauses and variable spectral content, it would be a waste to allocate a fixed bit rate to the audio channel. Instead, Phylon's system lets the data channel take advantage of the pauses and other gaps in the audio channel by dynamically varying it's bit rate between 4.8 to 19.2 kbits/s.

It should be noted that this dual-channel system isn't limited simply to carrying voice data. Once a second path is established, it can be used to carry any type of digital information, such as MIDI-channel sound-synthesis data, video information, or even sensor data and control signals for robotic functions.

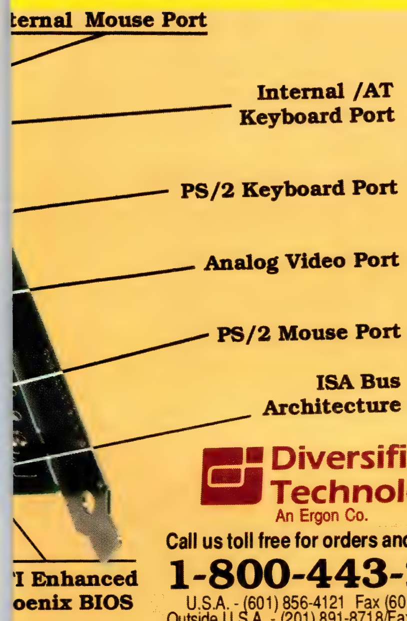
SOFT UPGRADES AHEAD

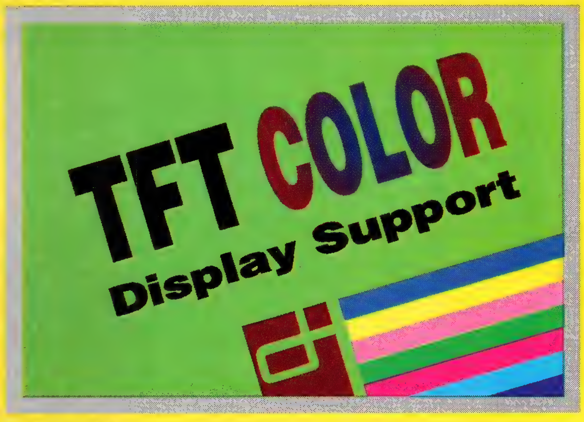
Those who are forced by market pressures to commit to a particular simultaneous voice/data technology before a standard is established needn't worry. Since most of the new modem chips use software-driven controllers and DSP circuits, it may be quite easy to upgrade existing equipment to support a common simultaneous voice/data scheme with a software change.

The same "soft" solution will probably be used to support early implementers of V.34 technology. The final draft of the protocol was only recently firmed up, therefore only AT&T is shipping a completely compliant chip set. Even with this final version, it will take some time for all manufacturers to sort out the subtleties of the V.34 standard and become fully interoperable with all vendors. Fortunately, the reprogrammable, software-driven technologies that enable this generation of communication devices will also enable their users to keep their equipment up-to-date in a world of rapidly evolving standards.☐

HOW VALUABLE?	CIRCLE
HIGHLY	548
MODERATELY	549
SLIGHTLY	550

Flat Panel
lay Support
Board Computer





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	TX26D52VC1CCA	640x480	Color TFT w/ Display Enable
	LMG9060ZZFC	1024x768	Dual Scan Monochrome w/o Accelerator
	LMG9100ZZFC	1280x1024	Dual Scan Monochrome
Kyocera	KCL6448DSTT	640x480	Color STN DD - 8 Bit
Matsushita	S804	640x480	Plasma
Sanyo	LCM5327-24NAK	640x480	4 Bit Pack STN Color
	LM-CK33-33-22NEZ	640x480	4 Bit Pack STN Color
	LCM5330	640x480	4 Bit Pack STN Color
	LCM-5941-24NAK	1024x768	Dual Scan Monochrome w/Accelerator
Sharp	LM64P80	640x480	Dual Scan Monochrome
	LM64P80 w/VRAM	640x480	Dual Scan Monochrom w/VRAM
	LQ9D011	640x480	Color TFT w/ Display Enable
	LQ10DH15	640x480	Color TFT w/ Display Enable
	LQ9D011	640x480	Color TFT w/o Display Enable
	LQ10DH11	640x480	Color TFT w/o Display Enable
	LM64C031	640x480	Extended 4 Bit Pack STN Color
	LM64C08	640x480	Color STN DD - 16 Bit
	LJ64ZU50	640x480	EL
Toshiba	LTM09C015-1	640x480	Color TFT w/ Display Enable

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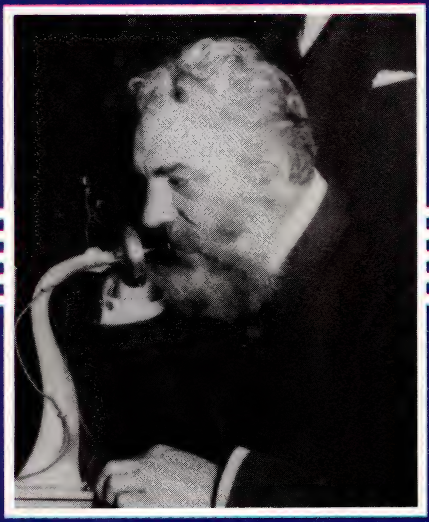
YOU DON'T HAVE TO BE



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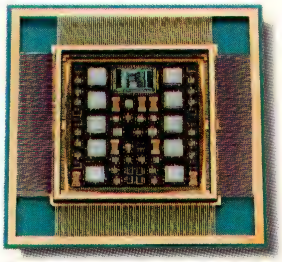

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VERTICAL INTEGRATION OF SILICON ALLOWS PACKAGING OF EXTREMELY DENSE SYSTEM MEMORY IN TINY VOLUMES.

MEMORY-CHIP STACKS SEND DENSITY SKYWARD

DAVID MALINIAK

Many aspects of board design, such as timing, thermal issues, and manufacturability, require innovative thinking. But if there's one aspect of board design that's relatively predictable, it's the layout, which is done in the X and Y dimensions. Chips are, almost without exception, placed side by side in some arrangement, even if the board is double-sided or flexible.

This constant of board design, however, is the great limiter of a board's packaging density. And nowhere is this limitation more glaring than in the layout of system memory, where row upon row of DRAMs sprawl across vast expanses of pc board like some silicon suburban development.

But the push is on to shrink systems, and the traditional layout concepts are becoming an extravagance. Over the years, there have been a number of attempts at exploiting the third dimension in board layout. Chips have been stood on their edges and sandwiched together and there have been attempts at stacking them vertically. But until now, such schemes have been either too expensive or the yields have been poor. In some cases, the density achieved wasn't worth the effort.

With the development of its technology for vertical integration of memory wafers, wafer segments, and individual die, Cubic Memory Inc. (CMI), Scotts Valley, Calif., has shattered the density barrier *(Fig. 1)*. Instead of the 40-to-80-Mbyte/in.^{3} storage densities possible with conventional packaging—using 16-Mbit memories in small-outline J-lead packages (SOJs) or two-sided thin small-outline packages (TSOPs)—CMI claims the ability to achieve densities of a gigabyte or more per cubic inch.

Stacking memory ICs vertically has other benefits besides the density gains. The close physical proximity of the chips significantly reduces the system delay associated with interconnect capacitance and pc-board trace length. Speed is increased while power requirements and operating temperatures are reduced compared with horizontal layouts.

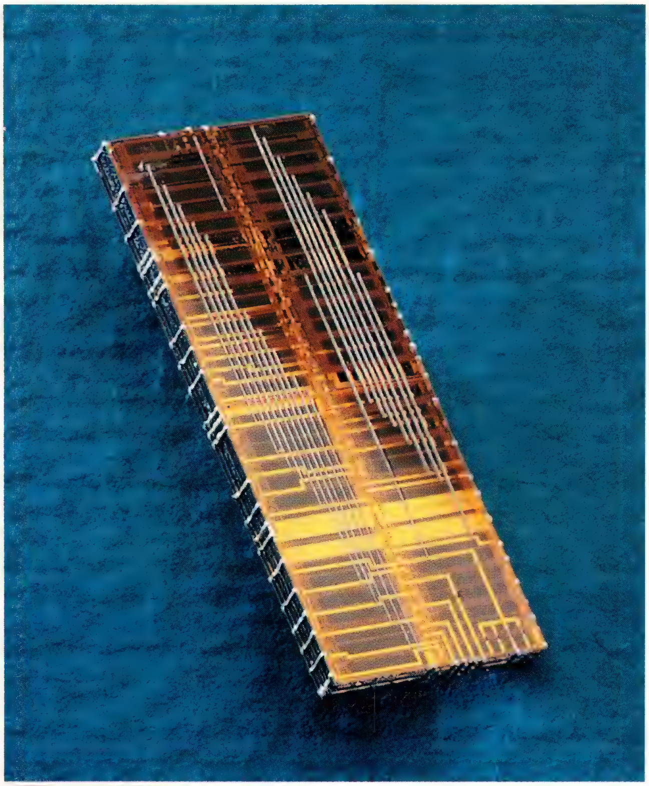
CMI has leveraged its chip-stacking technology into an initial pair of product families.

One takes advantage of the PCMCIA-card format for adding workstation-quantity memory to Pentium-based portables, while the other works within the DRAM SIMM format. Both merely hint at the technology's potential, which is not necessarily limited to stacking of memory alone.

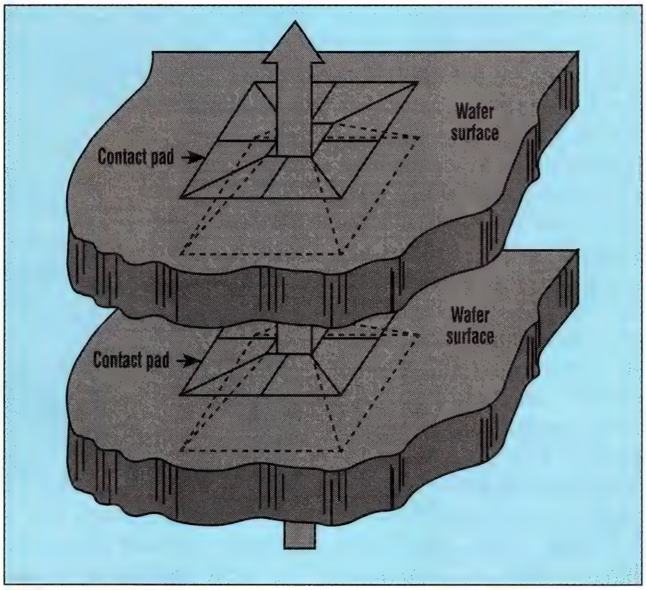
There are actually three separate technologies for vertical integration, each of which is suitable for different applications. The three processes are referred to as the large-hole process, the small-hole process, and the Vertical Interconnect Process (VIP). Common to each process is a vertical silicon interconnect and a patented compliant interconnect scheme.

The first two processes, known as the large- and small-hole processes, use a patented, pyramid-shaped via through the silicon *(Fig. 2)*. The small opening on the top of the pyramid penetrates on the circuit side and the large opening comes through the back side of the silicon, where the interconnect makes contact with a number of circuit elements on the silicon immediately below. This interconnect method takes up no space, as all pins fan out under the silicon stack instead of taking up large areas around the perimeter of the active silicon, as is done with conventional packaging. In addition, this method allows the individual circuit elements to be easily isolated for testing up until the final stack assembly.

The VIP process is a less expensive extension of the small-hole process and does not require the pyramid-shaped via through the silicon. Instead, gold interconnect traces and vertical-interconnect pads are deposited over insulating layers of polyimide. The gold traces provide horizontal interconnection of the die on a single layer or segment, and the gold pads provide a non-oxidizing metal surface for the layer-to-layer interconnections.



1. INSTEAD OF THE 40-to-80-Mbyte/in.^{3} storage densities possible with conventional packaging (using 16-Mbit memories in SOJs or two-sided TSOPs), Cubic Memory Inc. (CMI) claims the ability to achieve densities of a gigabyte or more per cubic inch.



2. BOTH THE small- and large-hole processes use a pyramid-shaped via through the silicon to make the vertical interconnections. The small opening on the top of the pyramid penetrates on the circuit side and the large opening comes through the back side of the silicon, where the interconnect makes contact with a number of circuit elements on the silicon immediately below.

Whole wafers, segments of wafers, or individual die can be stacked. In addition, multiple silicon technologies can be mixed in the same stack *(Fig. 3)*. Other components can be placed on top of the silicon stack as well.

For the small-hole and VIP processes, standard wafers can be used without need for any custom silicon. Individual chips can be selected by the control circuitry. The vertical chip-to-chip distance is variable from 0.003 to 0.010 in., depending on the application and density required.

The vertically integrated stacks are attached directly to pc boards. Tests on whole wafers and wafer segments have shown a 15% reduction in power consumption and a 20°C lower continuous operating temperature when compared to identical circuits operating in conventional plastic packages.

Originally, the large-hole process was developed to allow stacking of complete 6-in. DRAM wafers. The pyramid-shaped holes are filled with a mesh of fine gold-plated wire. The wires form a mushroom shape on the circuit side of the wafer, and the other ends of the wire are compressed and contained in the pyramid base. When the wire-filled base of the pyramid of one wafer is brought into contact with the top of another wafer, the mushroom-shaped "fuzz button" is captured by the base of the pyramid. All of the wires are then contained and a compressive gold-to-gold contact is formed between the circuit elements of both wafers. The result is a very reliable, fully compliant, reworkable interconnect that supports interconnections in both the horizontal and vertical directions.

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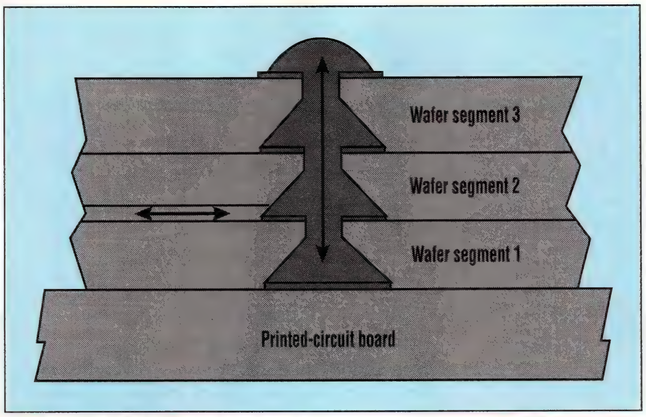
The "fuzz-button" interconnect does, however, require a custom mask set. And the holes are large by semiconductor standards: 150 μm at the top and 1000 μm at the base. This interconnect technology is still used in some applications.



3. WHOLE WAFERS, segments of wafers, or individual die can be stacked. In addition, multiple silicon technologies can be mixed in the same stack. Other components can be placed on top of the silicon stack as well.

The small-hole process was developed as a refinement of the large-hole, "fuzz-button" technology to allow interconnects on standard semiconductor-die bonding pads without the need for a specialized structure. In this method, off-the-shelf memory wafers can be used without the need for the semiconductor manufacturer to run a custom mask set.

In this case, the hole-making process is similar to the fuzz-button process, but the dimensions change. The wafers are thinned and the holes are small enough (25 μm on top, 120 μm on bottom) so that the vertical interconnect is accomplished within a bond-pad area and on conventional bond-pad pitches.

The small-hole process incorporates one level of discretionary wiring for every layer of silicon in the stack. Each die also has the necessary control signals brought out so that the control circuitry can address each chip uniquely.

Silver-filled epoxies are used for the compliant conductive material. These proven materials are the same ones that have been used for years by semiconductor manufacturers as a die-attach medium. CMI has developed a proprietary application method for the dispens-

PUTTING MEMORY STACKS TO WORK

Manufacturers of laptop/notebook computers are forever facing the challenge of squeezing desktop performance into an easy-to-transport package. In the RISC-workstation arena, the problem intensifies, because many of the Unix-based applications demand tremendous amounts of memory to execute quickly.

Just such a problem was faced by designers of the SPARCbook III at Tadpole Technology plc, Cambridge, U.K., explains George Grey, the group chief/ executive officer. The need for an alternative to the standard DRAM single-in-line memory module (SIMM), which peaks in capacity at 32 Mbytes, led Tadpole to team with Cubic Memory Inc. (CMI) to develop higher-density SIMMs.

By taking advantage of CMI's vertical interconnect process (VIP), designers at Tadpole and CMI defined an extension to the standard DRAM SIMM that will initially provide 64 Mbytes of storage (organized as 16 Mwords by 36 bits, which includes byte-parity bits). Furthermore, CMI expects to double the capacity to 128 Mbytes per SIMM by late 1994, and still keep the SIMM height to just 1 in.

One of the first steps designers had to take to enhance the SIMMs was to expand the address range. They added one more address line and two additional row-address-strobe (RAS) lines by using several pins that were previously no-connect pins on the SIMM. Some of the key issues that designers had to deal with, explains Dave Pedersen, V.P. of engineering at CMI, included the banking architecture and capacitive loading effects in highly-configured systems. Fortunately, because the memory chips are mounted on top of each other, there are no package loading effects. Also, typically, only one bank of memory is turned on at a time, which minimizes thermal problems.

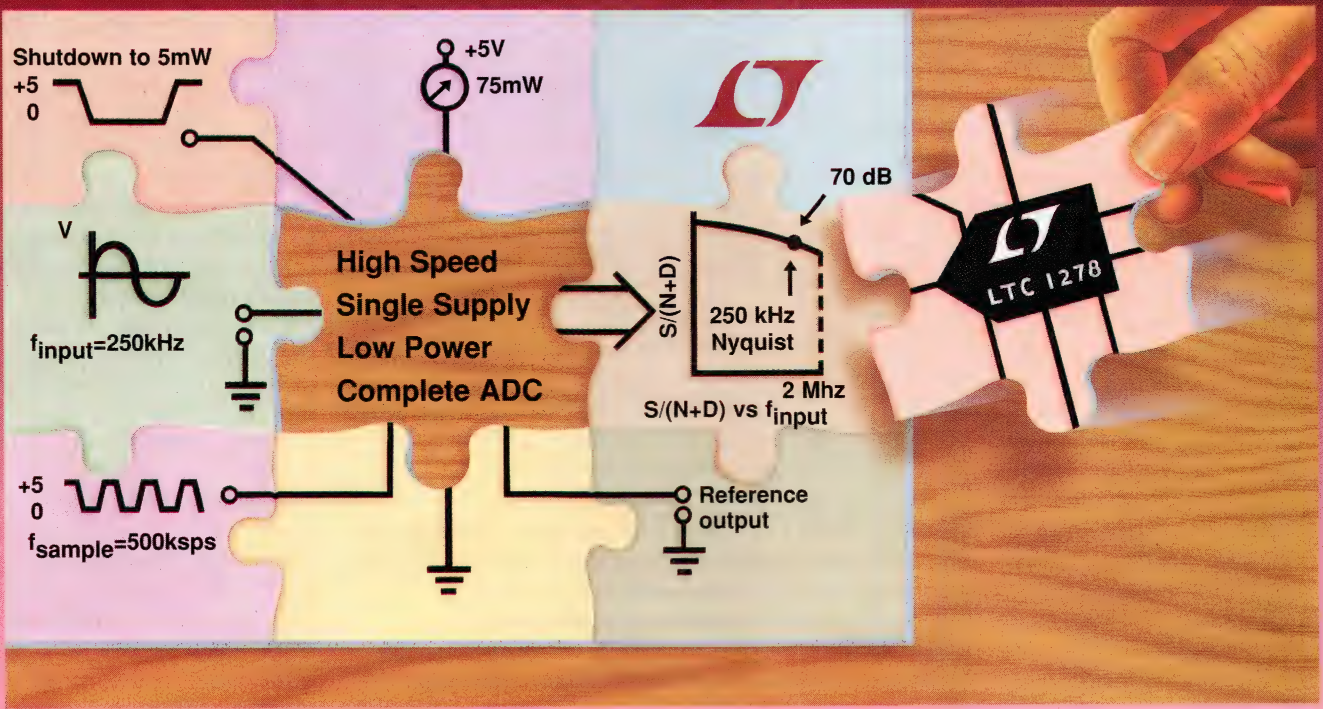
Once the interface was defined, the memory structure was implemented using "stacks" of memory layers. The memory stacks consist of eight-segment layers (each segment can be thought of as a 2-Mword bank of DRAM). The VIP scheme employs pyramid-shaped recesses on the outer edge of the chips. Then, when the chips are stacked, the contact edges are exposed so that conductive epoxy easily fills the recesses and realizes the connections.

Each segment layer in the memory stack consists of a monolithic piece of silicon that contains four 2-Mword-by-8-bit DRAMs, thus forming a 32-bit-wide memory block. Complementing the 32-bit-wide stack is a second stack that provides the four parity bits for each word.

After the stacks are assembled, they are mounted in the SIMM substrate. The substrate actually has a hole the size of a stack cut into it and the stack is then inserted into the substrate. The stack protrudes out of one side of the substrate by the amount of the difference in their thicknesses. In the case of the 128-Mbyte stacks, which stand 0.160 in. tall, they protrude 0.098 in. from the 0.062-in.-thick substrate. That's less than the height of a thin small-outline package. When coated with the sealing epoxy, the mechanical durability of the SIMMs is as good as previous-generation SIMMs that were populated with surface-mounted components.

BY DAVE BURSKY

The Missing Piece To Your A/D Converter Puzzle.



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LTC1273	300ksps	70dB	5V	75mW	11.75
LTC1275/76	300ksps	70dB	±5V	75mW	11.00
LTC1278	**500ksps**	**70dB**	**5V or ±5V**	**75mW 5mW***	12.85
LTC1282	140ksps	68dB	3V or ±3V	12mW	13.47

*power down mode

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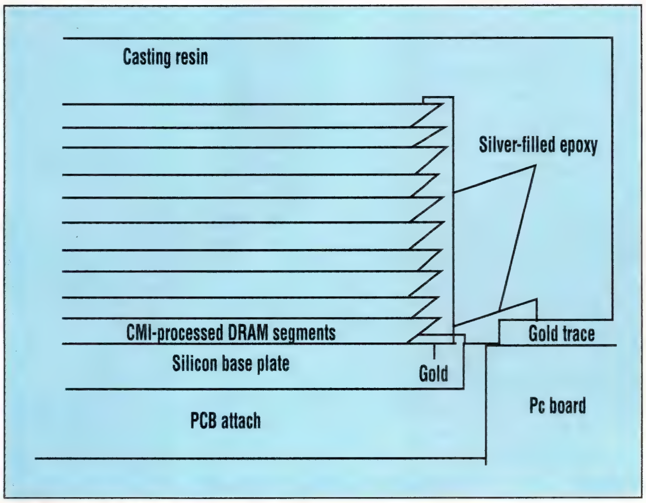
ing and application of these epoxies for connection in both the horizontal and vertical dimensions.

Taking the process a step further, the VIP process makes high-volume automation a part of the manufacturing cycle. It's also the lowest-cost method, because it uses a subset of the steps used in the small-hole process and does not require the pyramid-shaped hole through the silicon. The VIP process is suitable for stacking die and wafer segments that do not have a large number of interconnects to outside logic. It is not suitable, however, for stacking whole wafers.

In the VIP process, gold traces and vertical-interconnect pads are deposited over insulating layers of polyimide. Then, the wafers are thinned and sawed into segments. The segments' edges are beveled to allow vertical interconnection *(Fig. 4)*. The gold traces provide horizontal interconnection of the die on a single layer or segment and provide layer- or segment-specific memory-address decoding capability.

Pins that are parallelable are connected that way, which results in a reduction of pin count per layer of about 4:1. If the resulting stack has ten layers, the overall reduction in pin count is about 40:1. The gold bonding pads are exposed at the sides of the segments thanks to the 45° bevel cut and are used for the layer-to-layer connections.

A conductive silver-filled epoxy is used for both physical and electrical connection of the layers. The same conductive epoxy is used to connect the stack to the pc board. The stack is then encapsulated with a casting resin to provide protection and mechanical durability. The resin also provides some degree of thermal conductivity to enhance dissipation of heat from the stack.



4. IN THE VIP PROCESS, gold traces and bonding pads are deposited over insulating layers of polyimide. Then, the wafers are thinned and their edges beveled to allow vertical interconnection. The gold traces provide horizontal interconnection of die on a single layer or segment and provide layer- or segment-specific memory-address decode capability.

5. IN BOTH THE 88-pin JEDEC module and the SIMMs, the memory stacks are not mounted to the card's internal pc board as such. Rather, they are "floated" inside holes that go through the board and attached at their periphery by means of beam-style leads consisting of conductive epoxy. They are then glob-top-encapsulated on the reverse side to provide stability.

To leverage its chip-stacking technology into products that are usable today, CMI is offering two forms of memory modules for expansion of portable-system memory. One is the 3DMemory family of 88-pin JEDEC memory modules in capacities of 16, 32, 64, and 128 Mbytes. These are targeted for use in portables with a Type I PCMCIA slot, and are especially meant for Pentium-based portables that are expected to be able to address 64 Mbytes of system memory or more by this fall's Comdex show.

In this implementation of the technology, a glimmer of its potential impact comes into focus. For manufacturers using conventional technologies, volumetric space requirements limit portable add-in memory cards to one double-sided pc board using TSOP packages. Typically, only 16 to 18 ICs will fit into the available space, so to realize the maximum 16 Mbytes of storage, the manufacturer must use costly 16-Mbit DRAMs. Here's where the vertical-integration technology comes in. With it, memory cards are built using the most cost-effective DRAMs available. The 16-Mbyte card contains two stacks of four layers each. Each 2-Mbyte layer is made up of four 4-Mbit DRAM die. The 32-Mbyte card increases the two stacks to eight layers each. This produces a 16-Mbit module with a 32-bit word. Up to 128 Mbytes is easily accommodated within the PCMCIA Type I form factor.

For memory-card manufacturers using conventional packaging technologies, the volumetric space requirements limit the cards to one double-sided pc board using TSOPs. Only 16 to 18 memory chips fit into the available space, so to realize the maximum 16 Mbytes of storage, the manufacturer must use costly 16-Mbit

DRAMs. In contrast, CMI's vertical integration technique offers its inherent density advantages and enables cards with capacities of 16 Mbytes and more to be built using 4- or 16-Mbit DRAMs.

An interesting note on the construction of the cards is that the memory stacks are not mounted to the card's internal pc board as such. Rather, they are "floated" inside holes that go through the board and attached at their periphery by means of beam-style leads consisting of conductive epoxy. *(Fig. 5).*

For adding system memory to workstations and servers, CMI is offering a line of 3DMemory 64- and 128-Mbyte DRAM SIMMs. Previously, the maximum density of standard 72-pin SIMMs has been 32 Mbytes *(see "Putting memory stacks to work," p. 57).*

The 64-Mbyte SIMMs are made from eight layers of 8-Mbyte wafer segments (each made from four 16-Mbit DRAM die) plus a four-layer stack of 16-Mbit die for parity. The 128-Mbyte SIMMs will use 16 8-MByte layers, plus an eight-layer stack of 16-Mbit die for parity. The memory organization is 16 Mbytes by 36 bits for the 64-Mbyte SIMM and 32 Mbytes by 36 bits for the 128-Mbyte version.☐

PRICE AND AVAILABILITY

The 3DMemory 88-pin JEDEC memory modules will be sold to OEMs as well as through the reseller channel to end users. The 16-Mbyte modules are scheduled to ship in September, and at today's memory prices will have a suggested price of $995. The 32-, 64-, and 128-Mbyte versions will be available during the fourth quarter and pricing is projected at $1995, $3995, and $7995 each, respectively.

The 3DMemory 72-pin SIMMs will initially be sold only to OEMs. At today's memory prices, the 64-Mbyte SIMMs will cost $3999 in sample lots and $3599 in quantities of 1000. The 128-Mbyte SIMMs will sell for $7999 (samples) and $7199 (production quantities). Samples are available now and production quantities will be available during the fourth quarter.

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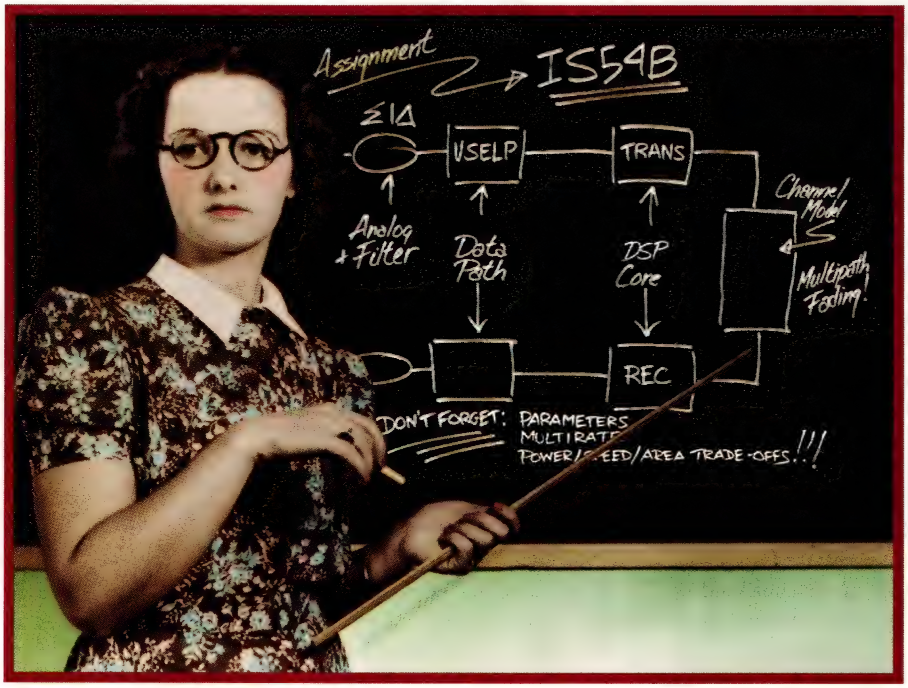

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BUILD A POWERFUL HOST-DSP INTERFACE

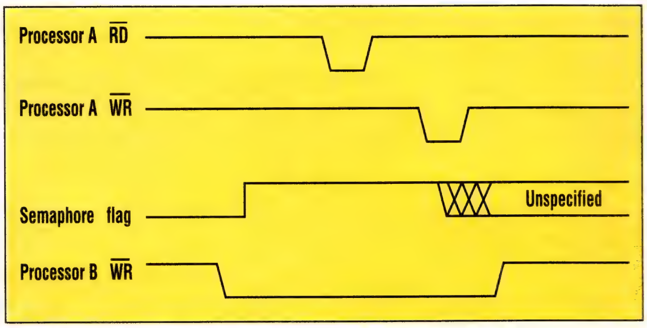
DUAL-PORT MEMORY COMBINES THE EASE AND COST OF FIFOS WITH THE DATAPATH CAPABILITY OF CUSTOM HARDWARE.

Digital signal processors (DSPs) are built to perform signal-processing functions. Voice signal-processing functions, such as modems, sound cards, speech compressors, and cellular telephones already use DSPs. Advanced signal-processing functions, such as image compression, speech recognition, optical character recognition and video conferencing will become commonplace as DSPs become more powerful and less expensive.

Whenever these signal-processing functions need to communicate with a host processor, interface hardware needs to be placed between the DSP and the host processor. The design complexity and cost of this interface hardware is usually more than that of the DSP itself.

High-volume DSP applications, such as modems and sound cards, integrate the interface hardware into an ASIC. Lower-volume and general-purpose DSP applications, though, can't justify the cost of custom hardware. These applications frequently use expensive discrete hardware solutions or inexpensive serial ports and FIFOs.

Unfortunately, for most applications, serial ports and FIFOs create unacceptable software complexity when the host-DSP interface requires several paths of information. A typical host-DSP interface, for example, may require a primary datapath, a diagnostics datapath, and a control/status datapath.


Processor A $\overline{RD}$
Processor A $\overline{WR}$
Semaphore flag
Unspecified
Processor B $\overline{WR}$

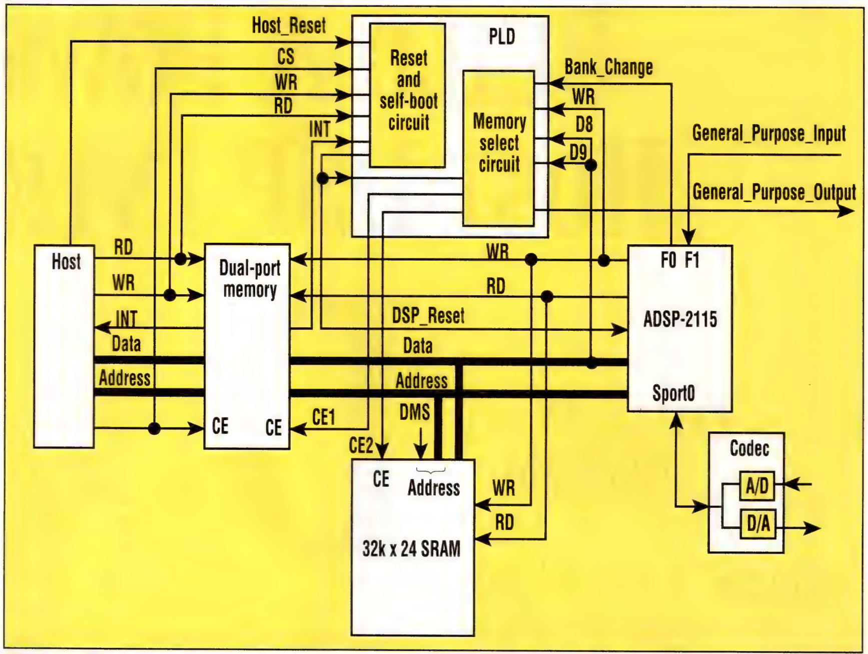
1. DUAL-PORT MEMORY SEMAPHORE-flag clash can occur when a faster processor responds before the slower processor finishes its initial write cycle. This can be avoided by adding wait states or strategically resequencing the I/O instructions in the faster processor.

A new design technique using a dual-port memory combines the design ease and low cost of serial ports or FIFOs with the multi-datapath capability found only in custom hardware *(see "Vocal Technologies' DSP solutions," p. 80)*. The design technique is based upon a dual-port memory feature previously unrealized by the device's manufacturers. Use of this design technique allows DSPs to be used in applications formerly enjoyed by only ASIC based high-volume designs.

Dual-port memories provide random access to a common memory through independent address and data lines. The dual-port memory concept has been around since the first computers. In 1983, Synertek introduced the first integrated dual-port memory IC (the SY2130 and SY2131). Volume production of dual-port memory devices has since brought the once specialized IC in-line with commodity-part pricing.

The industry standard architecture can be seen in devices from Cypress Semiconductor and Integrated Device Technology (IDT). Several other manufacturers, notably Advanced Micro Devices (AMD), Motorola, and Dallas Semiconductor have dual-port memories with extended features. These features are often unnecessary.

MICHAEL DEMJANENKO
Vocal Technologies Ltd., Baird Research Park, 1576 Sweet Home Rd.,
Buffalo, NY 14228; (716) 688-4675.



2. A HIGH-THROUGHPUT DSP interface is implemented with low-cost dual-port memory. All of the required glue logic is contained within an inexpensive PLD.

The most common sizes for dual-port memories are either 1024-by-8 and 2048-by-8, but much larger sizes are available.

An important feature of standard dual-port memories is the interrupt capability. These devices have certain memory locations that are referred to as mailboxes. There is one mailbox for each direction of communication. The mailboxes are addressed as the top two memory locations of standard dual-port memories. For the Cypress CY7C130, a 1024-by-8 dual-port memory, these addresses are at 7FEH and 7FFH. When one processor writes to its mailbox, an interrupt is generated to the other processor. When the other processor reads that mailbox, the interrupt condition is cleared. Normally the contents of the mailbox indicates a command or response code.

An exchange of information through dual-port memory mailboxes may occur as follows:

1. Processor A writes several (or perhaps hundreds) of dual-port memory locations with information bound for Processor B.

2. Processor A then writes a command byte into its mailbox, called Mailbox B, generating an interrupt to Processor B.

3. Processor B, when interrupted, reads the command byte from Mailbox B. This read also clears the interrupt to Processor B.

4. Processor B services the information in accordance to the received command byte. Processor B may, in part, write response information back to Processor A through the dual-port memory.

5. Processor B writes a response byte into Mailbox A. The act of writing to Mailbox A causes an interrupt to Processor A.

6. Processor A then reads the response byte and any other information sent from Processor B.

Notice all information essentially goes through one channel, the mailbox locations. The interrupt capabilities of standard dual-port memories provide single-channel communication capability. The potential multi-channel capability of the dual-port memory using this classic technique can't be realized.

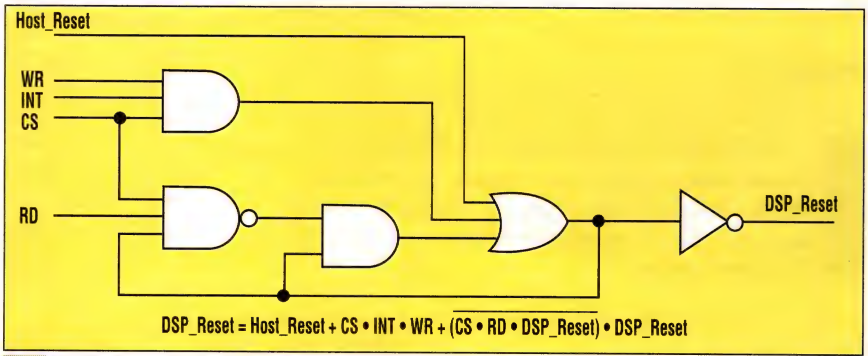
Like interrupt-driven techniques, inter-processor communication can also be supported with polled techniques. In fact, in certain instances, polling is preferable to interrupts. This is often the case with DSPs because they are frequently limited in their hardware-interrupt support. DSP software, due to real-time requirements, can often guarantee that a certain set of instructions are regularly executed. Installing polling routines at either the start or end of these repetitive DSP routines will not decrease the robustness of the communication channel. Often interrupts can be used in conjunction with polling, as will be discussed later.

Semaphore flags are a popular technique for passing information between two independent software processes. A typical semaphore exchange is as follows:

1. Processor A initially owns a block of memory. It writes into that block information that is bound to Processor B.

2. Processor A sets the semaphore flag; Processor B now owns that block of memory.

3. When Processor B sees the semaphore flag set, it will service the information and potentially write more in-


Host_Reset
WR
INT
CS
RD
DSP_Reset
DSP_Reset = Host_Reset + CS • INT • WR + (CS • RD • DSP_Reset) • DSP_Reset

3. RESET and self-boot circuitry inside the PLD controls the ADSP-21xx boot mechanism. When the DSP's reset is released, the ADSP-21xx automatically starts booting in code.

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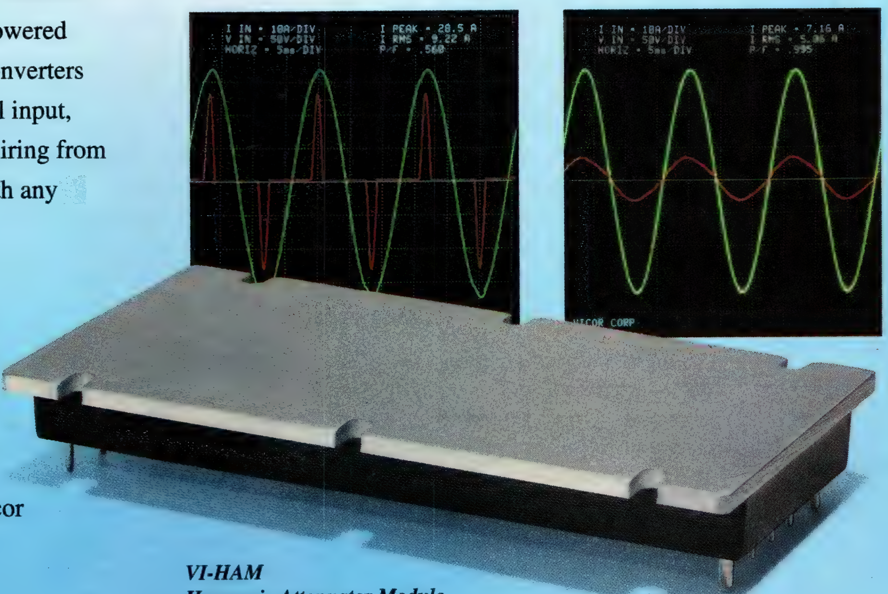

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READER SERVICE 139

formation into this block of memory.

4. After Processor B completes its services, it will clear the semaphore flag.

After this semaphore exchange, Processor A again owns the block of memory, and the cycle repeats. When semaphores require no special hardware, the number of semaphore channels are limited only by available memory.

Unfortunately, using semaphore techniques with dual-port memories is much trickier than with single-port memories. This is because with single-port memories, no more than one software process can read or write a particular location at one time. However, this is not the case with processors communicating through a standard dual-port memory.

A problem arises because the logic internal to most dual-port memories provides a "blocking" feature when two processors attempt to access the same location. When this situation occurs, the later processor's access will be blocked. Dual-port memories, such as the Cypress CY7C130, provide a Busy signal to both interfaces. When an access (read or write) by a processor is blocked, the appropriate Busy signal to the processor is activated.

When both processors access the dual-port memory simultaneously, it's unclear as to which of the two processors will be blocked. However, it's always guaranteed that one processor will succeed in its access, and the other will be blocked. The Busy is deasserted when the winning processor finishes its access. The purpose of the Busy signal is to hold off the losing processor's access.

If both processors simultaneously attempt to read from the same dual-port memory location, one of the Busy signals will be asserted. However, both processors will still read the correct value of the shared location. If both processors attempt to write to the same dual-port memory location, one of the Busy signals will be asserted, and that processor's write will be ignored while the other processor's write will be successful.

Two scenarios can occur if a processor attempts to read from a dual-port memory location while the second processor attempts to write to the same dual-port memory location. If the write cycle is blocked, the read will be successful in returning the current value of the location. If the read cycle is blocked, the write will be successful. The value then returned by the blocked read cycle is unspecified. Furthermore, this value may be different than both the previous and the new contents of the location.

For real designs, it's usually unrealistic to look at the Busy signal to determine if a memory-access cycle was successful. But there's no way around this when using conventional dual-port memories like the CY7C130. However, a new design technique using expansion dual-port memories circumvents the need to look at the Busy signal.

Expansion dual-port memories are required when dual-port memories are used on wider data buses. A single conventional dual-port memory provides the shared location memory arbitration and Busy generation. All other dual-port memories on the same data bus have Busy inputs that are connected to the conventional dual-port memories' Busy output. Expansion dual-port memories do not perform arbitration, but rather accept arbitration signals. The novel feature of the CY7C140 expansion dual-port memory is its actions when both Busys are tied inactive.

The CY7C130 conventional dual-

VOCAL TECHNOLOGIES' DSP SOLUTIONS

Vocal Technologies Ltd., designer of high-speed modems and other communications technologies, developed the low-cost, high-throughput interface described in this article for their embedded modems. As a DSP becomes a common resource on PC motherboards, complete modem software is increasingly required to coexist with other digital-signal-processing applications such as sound cards, image processing, and voice recognition.

Furthermore, the complexity of the modem software itself is growing. A modern data modem must implement over ten International Telecommunications Union (ITU-TS), formerly CCITT, and Bell data/facsimile modulations, offering throughputs from 300 bps to 14,400 bps and beyond. Among other requirements, modem DSPs must support DTMF generation, call progress detection (dialtone, busy, ringing), and several forms of voice compression.

The host controller of a modem implements error correction (V.42, MNP 1-4), data compression (V.42 bis, MNP 5), T.30 facsimile timing/control, facsimile command sets, and the standard AT command set. Future generations of modems will combine these functions onto the DSP as well.

Because the bulk of the host controller's time is spent compressing and decompressing, as well as building and tearing down error corrected packets, efficient dispatch is required to handle the high-throughput data interfaces. The host controller ideally processes the data in interrupts. When an interrupt occurs from the DSP, all semaphores are examined and the semaphores requiring service are noticed. Most semaphore servicing is done within the interrupt. However, some low-level monitor functions are scheduled to be performed by the background.

The DSP process in a modem is well characterized. The incoming and outgoing telephone line samples are at 7200 Hz (8000 Hz for digital lines). The main processing loop executes at this rate. It's convenient to examine all semaphore flags once in this loop. If any require servicing, the corresponding event is scheduled to occur. Because multiple channels can exist through the dual-port memory, this modem design is well suited for multitasking systems. Multitasking is an important characteristic because next-generation modem platforms are expected to support more than just modem applications.

port memory may block a write access when two processors are addressing a shared memory location. If the write represents a semaphore, then the semaphore would be lost. When used in this configuration, the CY7C140 expansion dual-port memory, on the other hand, guarantees that the write will be successful. Of course the read data may be corrupted, but as will be shown, this doesn't have to be a problem.

The definition of the semaphore must be limited. A semaphore flag stored in a dual-port memory location is defined to be False when the contents are zero, and True when the contents are nonzero. Both processors must be precluded from writing to the semaphore simultaneously. Furthermore, a processor is only permitted to write to the semaphore address when it is either changing the semaphore from True to False, or from False to True. All other writes to the semaphore, including overwriting with the same value, are prohibited. Because both Busy inputs of the CY7C140 are tied inactive, writes are guaranteed to never be blocked. Reads will never be blocked as well. However, the values read may be corrupted if the read occurs simultaneous to a write.

Due to the limited definition of our semaphore flag, the corrupted read value will be interpreted as either a True or a False. The value of the semaphore flag at the instant of any corrupted read must have been changing either from True to False or from False to True by the other processor. Because the corrupted value always corresponds to the correct value just prior to the write or just after the write, it's unimportant which value the semaphore is interpreted as.

It's possible that one processor is executing instructions at a much faster rate than the other *(Fig. 1)*. For example, Processor A may be an Analog Devices 2105 running at 10 MIPs (50 ns read-write cycle) and Processor B may be a PC's ISA bus (239 ns minimum read-write cycle). With such a disparity in bus speeds, the designer must ensure that the time from the faster processor reading the flag, through processing the information, to clearing the flag must be longer than the maximum write cycle duration of the slower processor. If this isn't the case, it's possible that the faster processor will try to clear the semaphore flag before the slow processor has completed its write cycle setting it! The state of the semaphore flag would then be indeterminate.

The ideal interface mechanism for DSP-host processor systems uses a combination of interrupt and polled techniques. The DSP polls the dual-port memory. Polling is appropriate because the processing requirements and structure of DSP algorithms are usually well defined. The host processor uses a combination of interrupt and polling. After the DSP changes the state of any semaphore, it will write to the mailbox address that generates an interrupt to the host processor. In the host processor's interrupt service routine, the interrupting condition is first removed by reading from the mailbox. The host processor then polls each semaphore flag. For every semaphore flag set, the host will schedule its service. The actual servicing may occur within the interrupt routine, or in a background process.

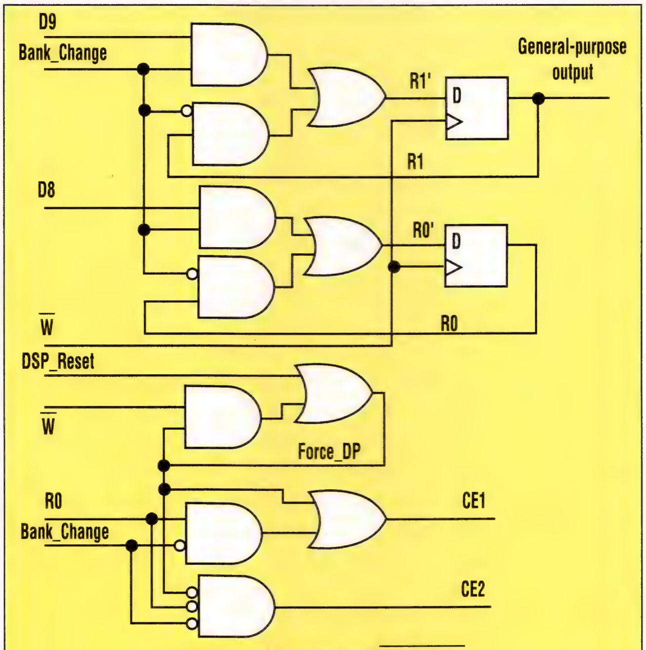
Interfacing a DSP to a dual-port memory is rather uneventful—it has the same interface signals as one would find on a standard SRAM. The Analog Devices ADSP-21xx family of processors provides a unique boot mechanism that can take further advantage of the dual-port memory *(see "Analog Devices' DSP family," p. 82)*. With the proper interface, no software is required to remain resident in the DSP system. All software can all be automatically downloaded from the host processor.

With the use of a low-cost PLD (such as a 15-ns 20V8), a versatile, low-cost, high-throughput DSP interface can be built that supports the ADSP-21xx boot mechanism *(Fig. 2)*. All of the required glue logic is implemented within the PLD. To complete the design, the external memory consists of three 32k-by-8 SRAMs. This fills out the complete data and program address space of the ADSP-21xx.

The ADSP-21xx self-boot mechanism is normally activated upon reset. This mechanism automatically downloads program code, one byte at a time, into the DSP's internal program memory. After the initial code is downloaded, it is automatically executed. The boot code may be downloaded from an external 8-bit wide ROM or from a dual-port memory.

The choice of a polled-DSP dual-port memory interface leaves the associated interrupt signal on the dual-port memory free for use in generating the DSP reset. The PLD is used to generate the reset signal to the DSP *(Fig. 3)*. Typically the DSP remains reset from power-up until the boot download procedure is ready to commence.

The host processor first writes the initial set of DSP startup instructions into the dual-port memory *(Fig. 2,*



$$R1' = D9 \bullet Bank\_Change + R1 \bullet \overline{Bank\_Change}$$
$$R0' = D8 \bullet Bank\_Change + Ro \bullet \overline{Bank\_Change}$$
$$Force\_DP = DSP\_Reset + Force\_DP \bullet \overline{W}$$
$$CE1 = Force\_DP + R0 \bullet \overline{Bank\_Change}$$
$$CE2 = \overline{Force\_DP} \bullet \overline{R0} \bullet \overline{Bank\_Change}$$

4. MEMORY SELECT CIRCUITRY inside the PLD selects either the SRAM, dual-port memory, or the internal PLD register. The memory map can be expanded by adding memory bank select bits to the internal PLD register.

again). This processor must read from any location in the dual-port memory to remove the reset signal to the DSP. Notice that a memory element is formed with combinatorial logic feedback that latches the reset signal until the host processor reads from the dual-port memory *(Fig. 3, again)*. Once the reset signal is removed, the DSP will begin to automatically download the startup instructions (boot) from the dual-port memory. After all of the startup instructions have been downloaded, the DSP will begin to execute them. The DSP must read its dual-port memory mailbox to clear the interrupt signal generated by the dual-port memory.

The host processor can reset the DSP at anytime by writing to the mailbox address twice. Any host processor write to the dual-port memory while the dual-port memory generated interrupt signal is active will cause the DSP reset to be asserted. The initial startup code downloaded by the DSP during the boot sequence then starts up a more sophisticated code/data download procedure.

Analog Devices' ADSP-21XX family of processors contain three memory-select signals. DMS is used to indicate data memory access cycles, PMS is used to indicate program memory access cycles, and BMS is used to indicate boot memory access. Only DMS is used in the design, and it's used to generate the most significant bit of address into the SRAMs.

Both program and data memory are contained within the SRAM. The assertion of either the RD or the WR signal from the DSP indicates the direction of memory access (read or write). It's important that the RD, WR, DMS, and PMS signals do not propagate through the PLD. That's because memory and dual-port memory access times are sensitive to any delays encumbered by these signals. The problem could be solved by the use of a faster PLD and memories, but this unnecessarily increases cost.

DMS does not propagate through the PLD in this design *(Fig. 4)*. Therefore, the propagation time of the PLD doesn't have to be fast. The access time of the SRAM is then solely a function of the clock in frequency (F) to the DSP. The following equation can be used to calculate the required speed of the SRAM:

$$T_{ACC} = 0.75(1/F) - 20 \text{ ns}$$

For an 11-MHz design, $T_{ACC} = 48.2$ ns, indicating that 45-ns SRAM would be sufficient. The speed of the SRAMs is only a function of the DSP clock, not any intervening logic.

The select signals to the dual-port memory and SRAM must be explicitly changed by setting or clearing a bit in a register internal to the PLD. During normal operating mode, either one or the other signal is active. In this design, when the ADSP-2115 flag output FO is set high, all external memory accesses are disabled to the dual-port memory and SRAM. During this interval, any external program or data memory write will write to the internal PLD register. Notice that all software associated with the changing of the contents

ANALOG DEVICES' DSP FAMILY

The Analog Devices ADSP-21xx family of digital signal processors (DSPs) offers modest memory space and processing power for relatively low-cost. These DSPs implement a modified Harvard architecture, which separates the internal program and data memory bus. This allows either an ALU, multiply-accumulate, or shift operation to occur in parallel with both a program memory and a data memory access.

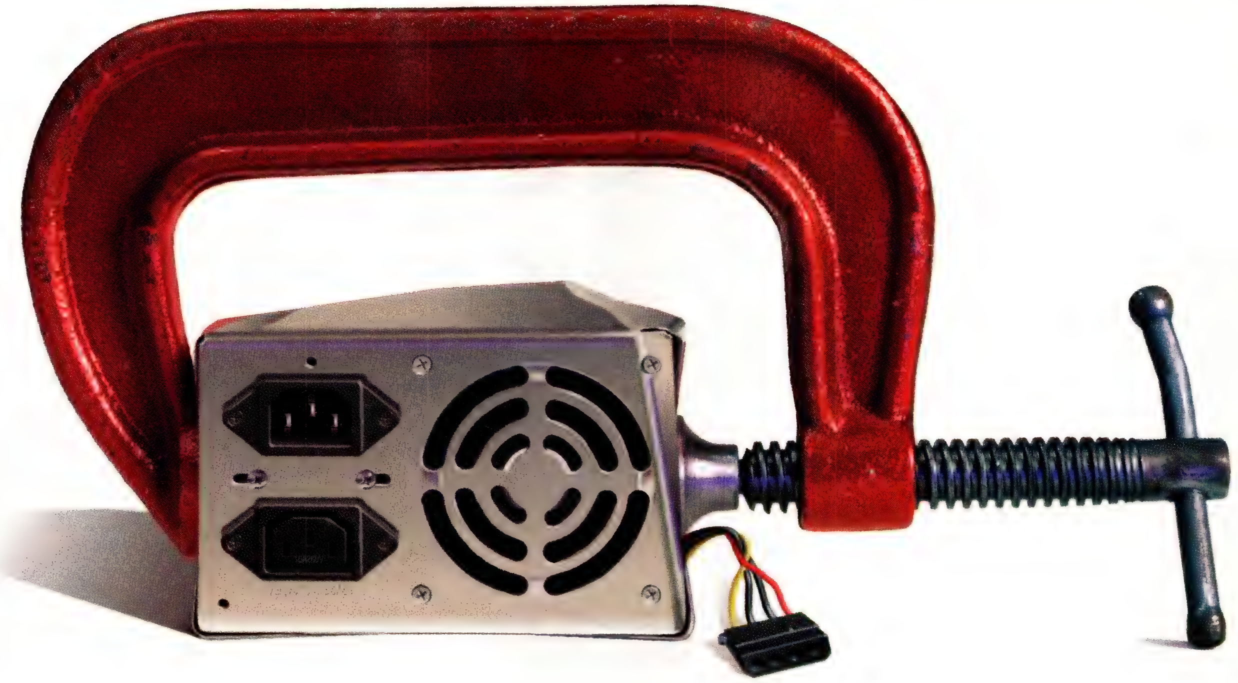
Because the program and data bus are multiplexed for external accesses, only one external access may occur per clock. This high degree of parallelism is controlled by a 24-bit program word. Each data memory word is 16 bits wide. The ADSP-2115 has 512-by-16-bit internal data memory and 1k-by-24-bit internal program memory. The address space of ADSP-21xx family is 16k words each of program and data memory.

The ADSP-21xx family provides a versatile boot-code download feature that can be initiated on reset.

```
   I0 = ^dual_port_buffer;
   I1 = ^dm_destination;
   M0 = 0;
   L0 = 1;     /* Auto increment pointers */
   SE = 8;     /* Shift count */
   CNTR = 500;
   AR = DM(I0, L0);     /* Read the first high byte */
   DO loop UNTIL CE;
    SR1 = DM(I0, L0);     /* Read each low byte */
    /* Combine high & low, read next high byte */
    SR = SR1 OR LSHIFT AR (HI), AR = DM(I0, L0);
loop: DM(I1, L0) = SR1;     /* Save word in data memory & loop */
```

To interface with inexpensive 8-bit memories, the ADSP-21xx downloads instructions eight bits at a time into its internal 24-bit program memory. The instructions are downloaded and automatically executed. These initial boot instructions usually boot in the rest of the digital-signal-processing software. When implemented through dual-port memories, this secondary boot mechanism can be quite efficient. With the reference design and a 10-MIP DSP, 500 16-bit words of data memory can be downloaded in about 300 µs *(see the figure)*.

Analog Devices' ADSP-2111 and ADSP-2171 do provide a direct host-controller interface on the DSP chip itself. This device connects directly to a host controller's bus. Four pins configure the interface for operation with different types of host processors. Interprocessor communication is accomplished through six data registers and two status registers. These eight registers are effectively dual-ported memory. Boot can be accomplished through this interface as well. This device is ideal for certain application because the entire host-processor interface is internal to the DSP. Communication realized though this interface are limited to single channel techniques.



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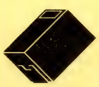	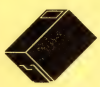	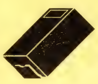	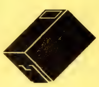		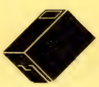		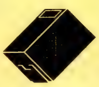		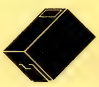	
6.3 V	10 V		16 V		20 V		25 V		35 V	
330 µF	220 µF	100 µF	100 µF	47 µF	68 µF	33 µF	33 µF	22 µF	22 µF	10 µF/15 µF
100 mΩ ESR	100 mΩ ESR	100 mΩ ESR	100 mΩ ESR	150 mΩ ESR	150 mΩ ESR	200 mΩ ESR	200 mΩ ESR	300 mΩ ESR	300 mΩ ESR	300 mΩ ESR
D case size = EIA 7343 E case size = EIA 7343H										

READER SERVICE 161

of the internal PLD register must be executed from internal program memory.

The state of the FO flag is unknown after DSP reset. However, the assertion of the DSP reset signal forces the dual-port memory select active by setting the signal Force_DP inside the PLD. Any succeeding external memory read by the DSP, such as in the boot sequence, will be forced to read from the dual-port memory. The first external write by the DSP will clear the Force_DP signal. This first write should be done with the Bank_Change signal off. A second write, this time with the Bank_Change signal asserted, should set the internal PLD register to a known state.

A spare registered output is provided within the design as a general-purpose output *(Fig. 4, again)*. Additional control bits and other features can be included by extending the internal PLD register to contain more bits. This can be used to provide additional output control bits. An almost limitless amount of memory can be made accessible by adding SRAM page select bits.

Although "jumping" between banks of memory may be cumbersome, this overhead is rather insignificant if each bank contains a separate task. The single flag input capability of the DSP can be expanded as well. The flag input (FI) can be driven by a PLD output. Inside the PLD, this bit could be a multiplexed signal of several PLD inputs. For a 2:1 multiplexor, the control could be the FO signal. For a larger multiplexor, several bits of the internal PLD register may specify the input to the multiplexor. ☐

Michael Demjanenko is a member of the technical staff at the Custom Product Design Div. of Vocal Technologies Ltd. His responsibilities include investigating and implementing various aspects of telecommunications products. He holds a BS and MS in electrical and computer engineering from the State University of New York at Buffalo.

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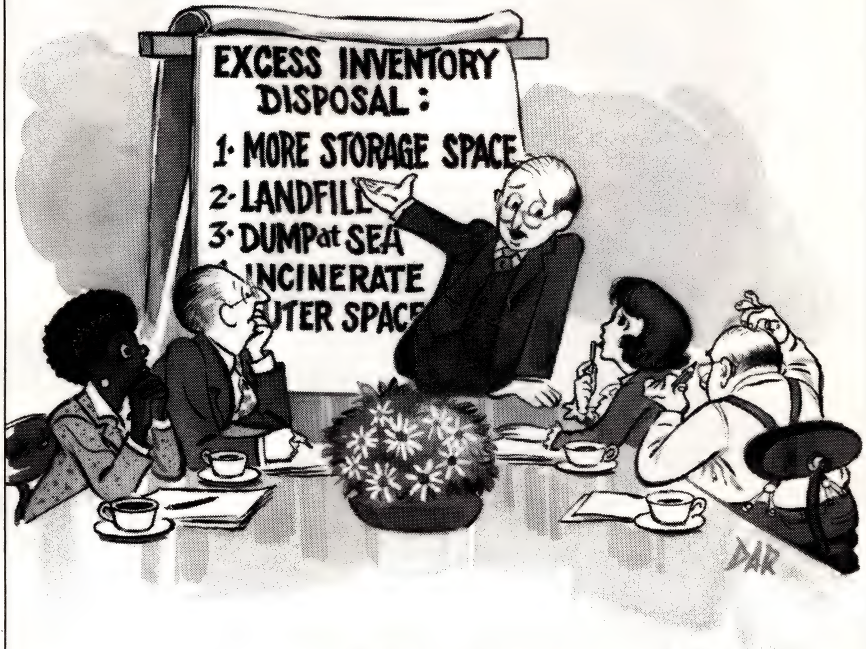

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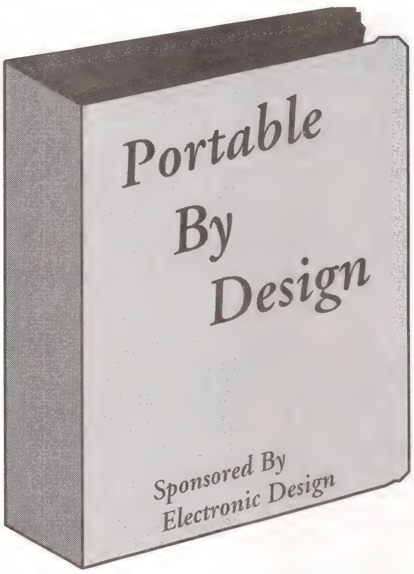

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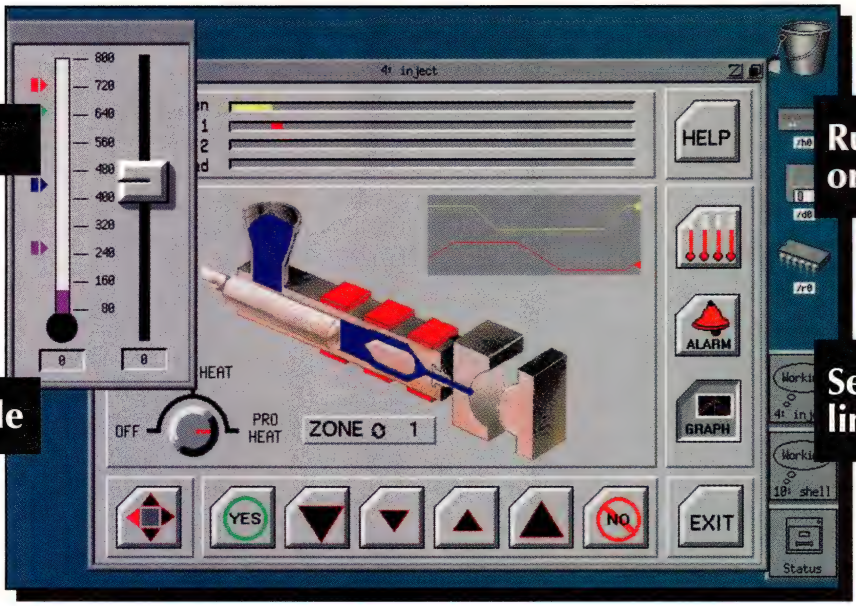

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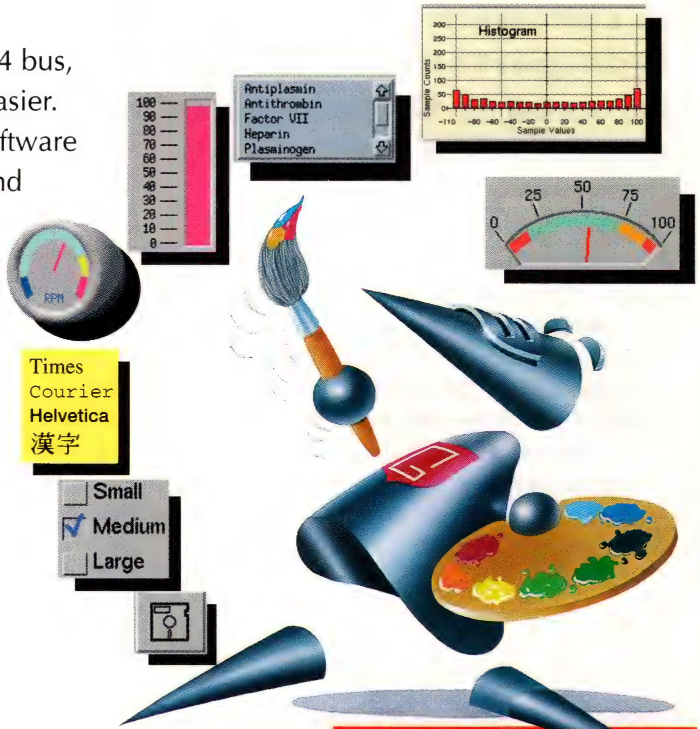

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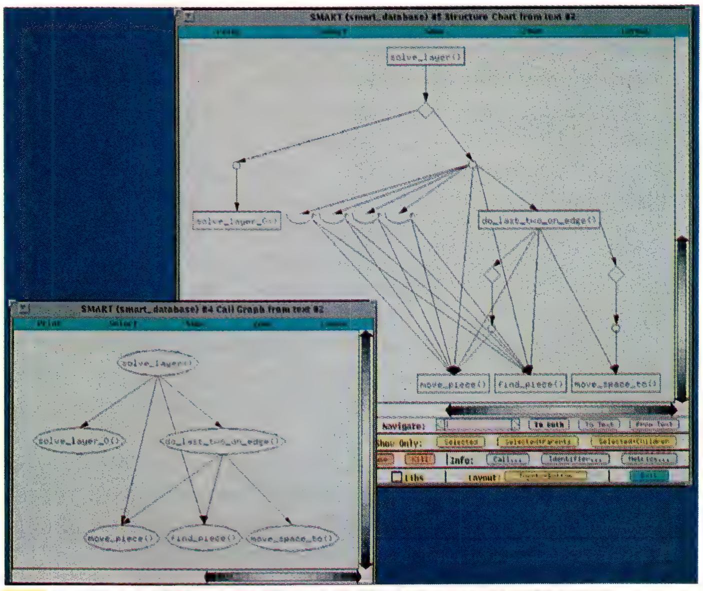
DEBUGGING SYSTEMS: GETTING THE PIECES TO WORK TOGETHER

FIXING ERRORS IN EMBEDDED SYSTEMS CALLS FOR TEAMWORK—AND TOOLS

SHERRIE VAN TYLE

When an embedded system fails, the story is that the engineers who designed the hardware and the developers who wrote the software point their fingers to the opposite camp. In reality, though, both groups would likely agree that debugging a design calls for teamwork, patience, experience, ingenuity, and perhaps most important—good tools. Indeed, the intersection between hardware and software is particularly dicey—how do engineers determine whether a problem is caused by hardware or software or is a result of their interaction?

To answer some of these questions, in a contributed article, Mark Call, senior development engineer at Storage Technology, discusses two areas of real-time debugging concerns faced when designing real-time systems: real-time software problems, such as error-recovery algorithms, and hardware integration problems, such as fault race conditions and physical positioning problems. In



1. PROCASE'S SMARTSTRUCTURE CHART shows code structure and control flow within individual functions. Each of the conditional elements shown in the structure chart can be used to navigate automatically to the corresponding decision point in the source code.

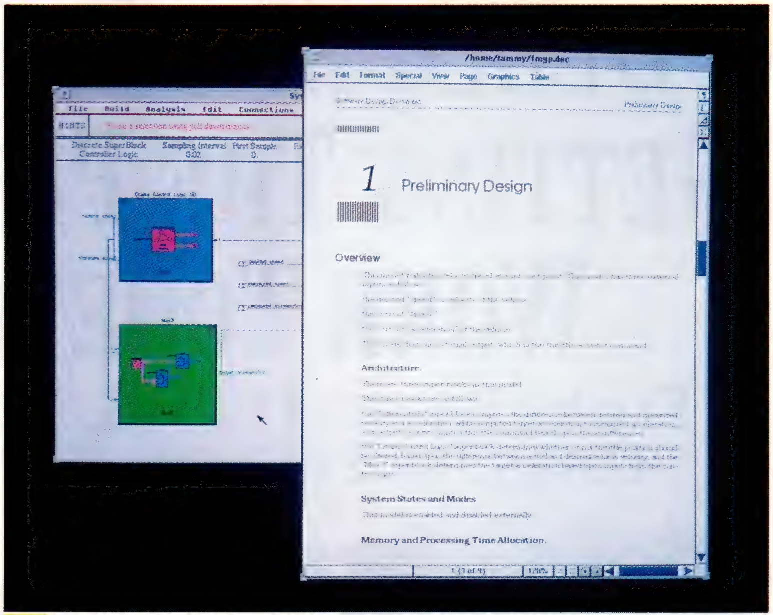
“Debugging: Enterprise Instrumentation,” (p. 93), Call draws on his experience working with 36-track tape drives; yet his debugging experience will likely sound familiar to engineers working on other high-end, real-time projects. For instance, problems may crop up quickly. What's more, they may happen only once. Also, large systems like these often require massive amounts of trace memory to find faults. As Call explains, the debugging tool set chosen for this project had to address several requirements that, though unique to the project, are examples of common requirements for a wide variety of real-time systems.

In the second contributed article, *“Debugging for Real-Time: Hard Choices,” (p.101)*, Ed Skinner, software developer and instructor with Motorola's Computer Group, focuses on picking the right tool for the system. Skinner takes a look at the range of available tools and their strengths and weaknesses: the programmer's tool set includes source-code debuggers, regression tests, system profilers, and firmware debuggers. He points out that choosing the best tool from the many varied toolsets at hand gives engineers the best shot at finishing their project on time and within budget.

The debugging picture is hardly bleak, however. Skinner describes the advantages of the new, inclusive development-and-debugging environments. Vendors are improving existing tools and introducing new toolsets. Recognizing that many engineers are now working in DOS/Windows as well as Unix environments, some vendors are either porting their toolsets to Windows or adding graphical user interfaces to tools. It's worthwhile to take a look at some common debugging issues and the tools that are aimed at solving typical embedded-system problems.

BEYOND THE BOUNDARIES

Debugging a system consisting of hardware and software requires expertise that goes beyond the boundary between the hardware and the software that drives it. Because software engineers are unlikely to debug hardware, any system-level problem that occurs usually falls to the hardware engineer to debug. This often requires the engineer to understand the source code that drives the hardware. Debuggers can be used to evaluate how the code is executing.



1 Preliminary Design

Overview

Architecture:

System States and Modes

Memory and Processing Time Allocation.

2. ISI's DOCUMENTIT PRODUCT GENERATES generates software documentation based on the company's Matrix$_X$ System Build block-diagram models. The documentation software simultaneously produces or changes the documentation as an engineer works on the model diagram.

For an engineer more comfortable with schematics than source code, debugging may not supply enough information. Understanding how source code is structured may give an engineer an idea of where the problem lies. To that end, Procase Corp.'s SmartStructure Chart and SmartReport Writer give engineers a view of the code's structure. The chart tool automatically generates a graphical representation of the code's structure *(Fig. 1)*. The graphic can serve as a schematic to help an engineer understand the code logic, as well as to see the decision points, control flow, and parameter usage. The chart tool used with SmartSystem code browsing and error analysis can help engineers navigate through the source code to the function call or decision point in question.

The writer tool automatically generates as-built documentation, ensuring that information used in debugging is up to date. Because the documentation is generated from the source code, the code and documentation are in sync. With these tools, once the hardware engineer has a sense of how the program logic is constructed, s/he can make informed judgments about the cause of the problem, make the fix, and then run a debugger to verify that changes made have had the desired effect.

Engineers coping with complex data-manipulation software should get a hand with CST Images' Data Debugging Toolset (DDT). The San Diego company's tools were developed to fill the gap between standard source-code debuggers and generic graphic toolsets. The tool supplies non-graphic, logic-based debugging controls to be embedded in a user program under development.

REMOTE X11 GRAPHICS

The toolset's routines generate remote X11 graphic displays with which the user can view program data results on a Sparc Unix host, control debugging flow, and analyze massive data arrays in graphical form. The tool targets analysis in general data processing, signal processing, and data acquisition. With the tool, the developer can insert debugging routine calls in the C and Fortran code at key points where data may be viewed and checked for algorithm verification. During debugging, calls are activated through switch parameters from the program/task, the toolset's graphic in-

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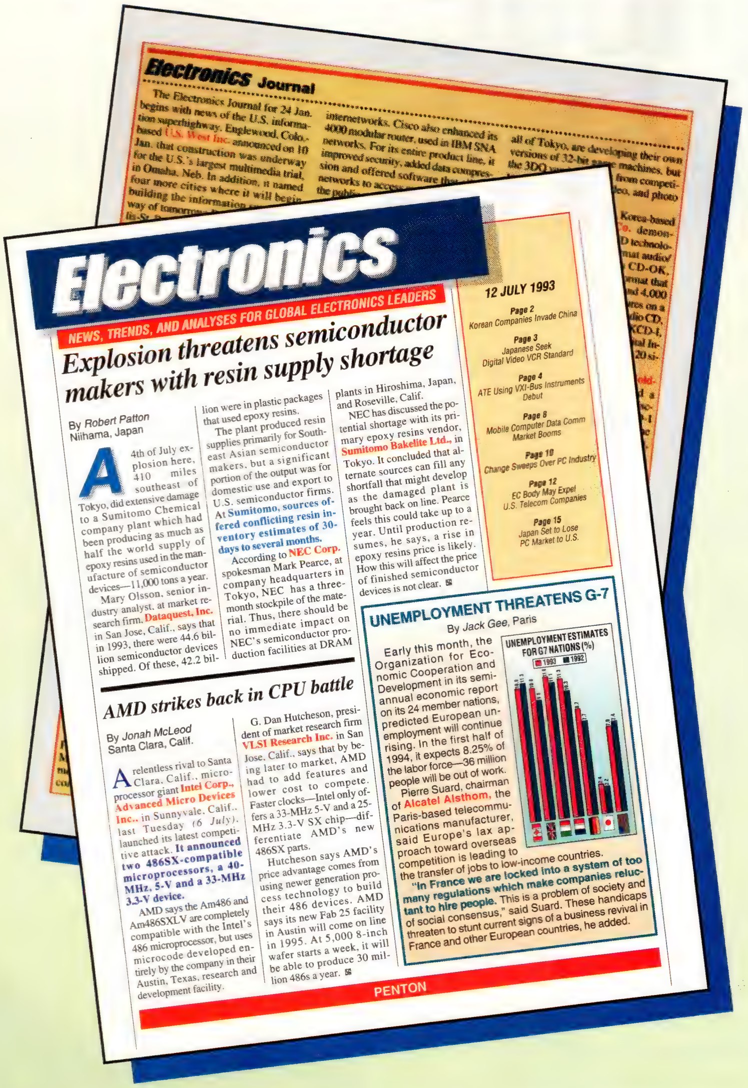

Electronics Journal

The Electronics Journal for 24 Jan. begins with news of the U.S. information superhighway. Englewood, Colo.-based U.S. West Inc. announced on 10 Jan. that construction was underway for the U.S.'s largest multimedia trial, in Omaha, Neb. In addition, it named four more cities where it will begin building the information

Electronics

NEWS, TRENDS, AND ANALYSES FOR GLOBAL ELECTRONICS LEADERS

Explosion threatens semiconductor makers with resin supply shortage

By *Robert Patton*
Niihama, Japan

A 4th of July explosion here, 410 miles southeast of Tokyo, did extensive damage to a Sumitomo Chemical company plant which had been producing as much as half the world supply of epoxy resins used in the manufacture of semiconductor devices—11,000 tons a year.

Mary Olsson, senior industry analyst, at market research firm, Dataquest, Inc. in San Jose, Calif., says that in 1993, there were 44.6 billion semiconductor devices shipped. Of these, 42.2 billion were in plastic packages that used epoxy resins.

The plant produced resin supplies primarily for Southeast Asian semiconductor makers, but a significant portion of the output was for domestic use and export to U.S. semiconductor firms. **At Sumitomo, sources offered conflicting resin inventory estimates of 30-days to several months.**

According to NEC Corp. spokesman Mark Pearce, at company headquarters in Tokyo, NEC has a three-month stockpile of the material. Thus, there should be no immediate impact on NEC's semiconductor production facilities at DRAM plants in Hiroshima, Japan, and Roseville, Calif.

NEC has discussed the potential shortage with its primary epoxy resins vendor, Sumitomo Bakelite Ltd., in Tokyo. It concluded that alternate sources can fill any shortfall that might develop as the damaged plant is brought back on line. Pearce feels this could take up to a year. Until production resumes, he says, a rise in epoxy resins price is likely. How this will affect the price of finished semiconductor devices is not clear.

AMD strikes back in CPU battle

By *Jonah McLeod*
Santa Clara, Calif.

A relentless rival to Santa Clara, Calif., microprocessor giant Intel Corp., Advanced Micro Devices Inc., in Sunnyvale, Calif., last Tuesday (*6 July*), launched its latest competitive attack. **It announced two 486SX-compatible microprocessors, a 40-MHz, 5-V and a 33-MHz 3.3-V device.**

AMD says the Am486 and Am486SXLV are completely compatible with the Intel's 486 microprocessor, but uses microcode developed entirely by the company in their Austin, Texas, research and development facility.

G. Dan Hutcheson, president of market research firm VLSI Research Inc. in San Jose, Calif., says that by being later to market, AMD had to add features and lower cost to compete. Faster clocks—Intel only offers a 33-MHz 5-V and a 25-MHz 3.3-V SX chip—differentiate AMD's new 486SX parts.

Hutcheson says AMD's price advantage comes from using newer generation process technology to build their 486 devices. AMD says its new Fab 25 facility in Austin will come on line in 1995. At 5,000 8-inch wafer starts a week, it will be able to produce 30 million 486s a year.

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Korean Companies Invade China

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Japanese Seek Digital Video VCR Standard

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ATE Using VXI-Bus Instruments Debut

Page 8
Mobile Computer Data Comm Market Booms

Page 10
Change Sweeps Over PC Industry

Page 12
EC Body May Expel U.S. Telecom Companies

Page 15
Japan Set to Lose PC Market to U.S.

UNEMPLOYMENT THREATENS G-7

By *Jack Gee*, Paris

UNEMPLOYMENT ESTIMATES FOR G7 NATIONS (%)
■ 1993 ■ 1992

Early this month, the Organization for Economic Cooperation and Development in its semi-annual economic report on its 24 member nations, predicted European unemployment will continue rising. In the first half of 1994, it expects 8.25% of the labor force—36 million people will be out of work.

Pierre Suard, chairman of Alcatel Alsthom, the Paris-based telecommunications manufacturer, said Europe's lax approach toward overseas competition is leading to the transfer of jobs to low-income countries.

"In France we are locked into a system of too many regulations which make companies reluctant to hire people. This is a problem of society and of social consensus," said Suard. These handicaps threaten to stunt current signs of a business revival in France and other European countries, he added.

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terface window, or source-code debuggers. If debugging operations are not active, the DDT calls impose low CPU overhead.

As for digital-signal processors, the AXDS multiprocessor and emulator and C source-level debugger from Ariel Corp., Highland Park, N.J., is based on Texas Instruments' XDS-510 but costs less than one third. Available for Ariel's Hydra and Cyclops C40-based DSP boards, the AXDS has a window-oriented user interface and includes an assembler, linker, and C source-level debugger. Other features include software breakpoint, trace, and timing with up to 30 software breakpoints, and hardware breakpoint and trace on all programs and data addresses.

For engineers working with DSP chips from NEC Electronics Inc., Mountain View, Calif., Intermetrics, Cambridge, Mass., has come up with an ANSI C cross-compiler optimized for the NEC MPD7701x family of DSP ICs. The compiler has language extensions to take advantage of the chip's architecture, including support for multiple memory spaces as well as access to circular buffer addressing modes.

OFF THE SHELF

Off-the-shelf multitasking kernels and real-time operating systems are proliferating. Many of them now include a kernel-aware debugger; yet the debugger does not deal with the target processor or the application's source code.

So that a user can avoid purchasing and having to learn to use two debuggers, Soft-Scope, a source-level debugger for 8086 family embedded-system development, has a set of macros for kernel and application awareness supporting the C Executive operating system from JMI Software Systems Inc., Spring House, Pa. From Concurrent Sciences Inc., Moscow, Idaho, SoftScope enables a user to access a task profiler that reports how much CPU time is used by each task, displays the amount of stack used by each task, displays system configuration information, and sets conditional breakpoints for a given task.

C Executive has Unix-like system calls, standard I/O with redirection, data queues for intertask byte streams, a reentrant C library, and a set of device drivers that support PC peripherals without using BIOS calls. A source-level, remote-target debugger that runs on DOS and Windows-based PCs, Soft-Scope supports C/C++ compilers from Borland, Intel, MetaWare, Microsoft, and Symantec.

From Microware Inc., Des Moines, Iowa, the FastFix Debugger is an ANSI C source-level debugger residing on the host system. With the debugger, users can remotely control program execution of the application while communicating with the OS-9 target system. The debugger supports C source-level and assembly language debugging and can simultaneously display C source and assembly code.

EMULATION, DOCUMENTATION

On the emulation front, the ET-iC186 unit from Emulation Technology Inc., Santa Clara, Calif., supports 16-bit microprocessors from AMD, Intel, NEC, Philips, and Siemens. The ET-iC186 supplies full-speed emulation up to 30 MHz with no wait states and no intrusion on I/O or interrupt pins. The clock source is switchable between the target system and the pc-board programmable oscillator.

In the race to debug a product and get it to market, design documentation often gets short shrift. To meet that need, as well as to help developers doing design reviews, software update and maintenance reports, user manuals, and version control, Integrated Systems Inc., Santa Clara, Calif., has added DocumentIt automatic documentation software to its Matrix toolset *(Fig. 2)* for developing embedded and control systems. Introduced with version 4.0 of Matrix, DocumentIt generates software documentation based on the tools' SystemBuild block-diagram models. As an engineer works on the model diagram, DocumentIt simultaneously produces or changes the corresponding documentation. The output is compatible with FrameMaker and Interleaf publishing software. ☐

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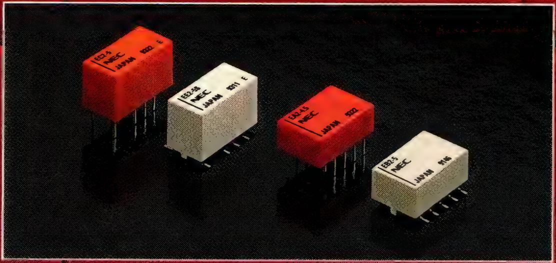

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DEBUGGING: ENTERPRISE INSTRUMENTATION

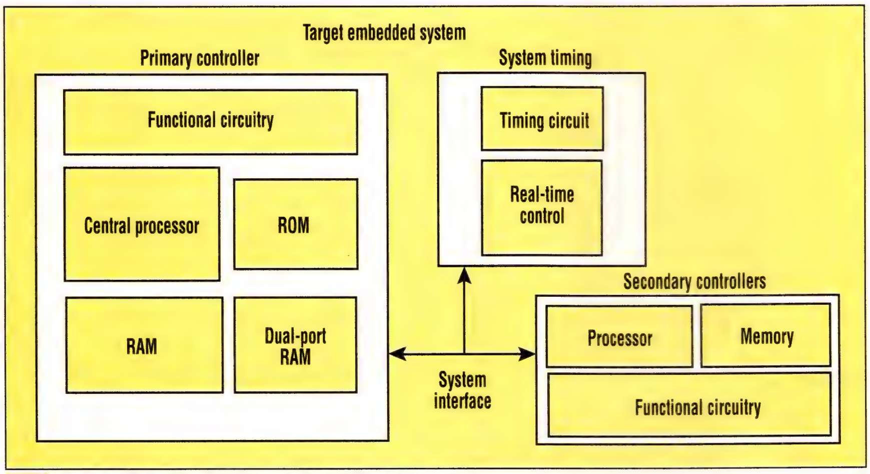
LOCATING REAL-TIME BUGS IN EMBEDDED SYSTEMS IS ESPECIALLY TRICKY WHILE INTEGRATING HARDWARE AND SOFTWARE

As embedded-system design engineers know, one of the more challenging stages in the development process occurs when it's time to integrate hardware and software in a real-time system. When bugs occur at this stage, it's often difficult to identify whether they are in the hardware or software or come as a result of their interaction. This article discusses two areas of real-time debugging concerns faced when designing real-time systems—real-time software problems, such as error-recovery algorithms, and hardware integration problems, such as fault race conditions and physical positioning problems *(Fig. 1)*.

The problems encountered when designing 36-track tape drives for IBM plug-compatible mainframes are similar to those faced on other high-end, real-time projects. Things may happen fast and perhaps only once. Such systems often require massive amounts of trace memory to track down the faults.

The debugging tool set chosen for this project had to address several requirements that, although unique to the project, are examples of common requirements for a wide variety of real-time systems. The target system processor was a Sparc-based CY611, the integer-only variant of the CY601 processor. The tool hardware interface had to support the CY611 without intruding on the target's real-time operation. The tool set must be flexible in its approach to a problem. Two teams of software engineers and one team of hardware designers were involved in the project. Members of other teams were involved occasionally. Both a hardware and a software approach to the problem had to be supported with good interaction between the tools.

The tool set must grow with the team requirements. Each of the three primary teams averaged a dozen members. While all members did not require simultaneous access to the systems, there was a strong requirement for massive data exchange and a consistent debugging environment between the team members and multiple debugging stations *(Fig. 2)*. The tool set chosen was the Microtec Research XRAY debugger with resident monitor and the Tektronix Enterprise DAS system analyzer operated jointly from a Solbourne S4000 workstation. This is a good model of an enterprise debugging environment.



1. REAL-TIME REQUIREMENTS can significantly increase the complexity of integrating an embedded system's hardware and software.

MARK CALL
Storage Technology Corp., 2270
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The tools are controlled from a common point. The digital analysis system (DAS) is networked to the workstation, and all debugging stations are networked for efficient operation and data exchange. The XRAY debugger is connected to the prototype via an RS-232 interface. Each DAS, 15 at last count, is attached to a prototype driving at least a portion of the product hardware. The system analyzer shows the designer what is happening on the bus in real-time. The debugger has the capability to run tests or interpret the system state after a breakpoint of failure. Similarly, the system analyzer can correlate specific hardware signals with the software instructions and correlate the debugger with the real-time trace.

REAL-TIME SOFTWARE

Tape drives are inherently real-time systems, because they control a high-speed electromechanical system, and they have the potential for multiple asynchronous events. In addition, performance requirements dictate a high level of custom integration—that is, dozens of ASICs in a single tape drive unit. The failing software module might be difficult to identify in real-time systems. Previous events and/or interrupt activity can cause the software to take radically different paths and process data in a different order.

The failure may be "hidden"—it may take several seconds to manifest itself and then may not be easily traced back to the source. Tape error recovery is a good example. Tape read or write errors, while not desired, are expected to occur occasionally, and may result from faults in either the drive, the media, or in the code, of course, especially during the debugging process. Since data integrity is paramount, extraordinary measures are employed to guarantee correct and recoverable data. The initial read or write problem that exercises the faulty software usually happens any number of tape repositions and retry cycles before the final error is detected.

Since these events can take seconds, or even minutes, to accumulate, the designer must both conserve the deep, but finite, trace memory and try to create trigger events ever closer to the original fault. Trapping the fault becomes an interactive, and often quite creative, process *(Fig. 3)*.

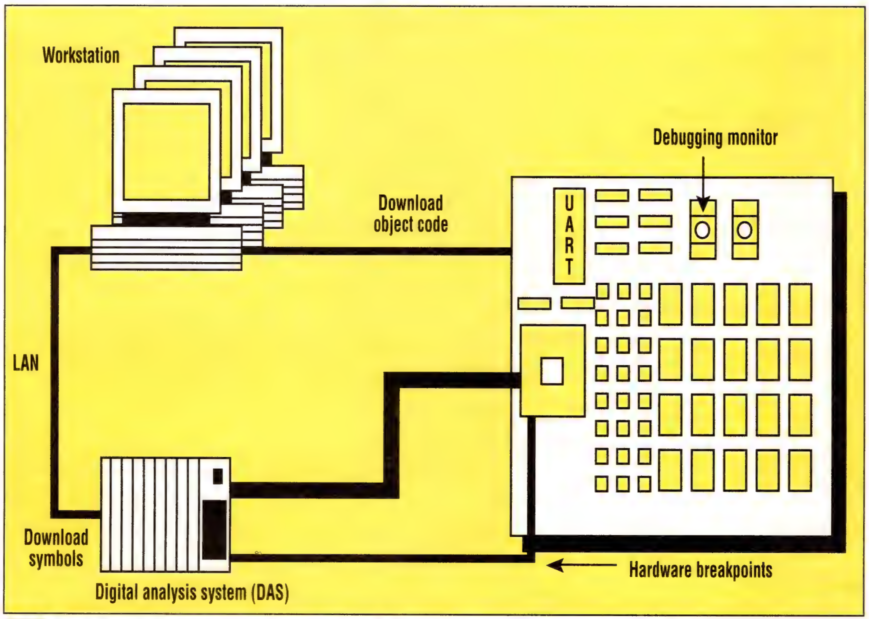
Generally, real-time systems cannot be stopped arbitrarily because signals or interrupts can be missed. In addition, electromechanical devices, such as tape drives, do not stop instantaneously when the code is stopped. The target must be allowed to continue to a reasonable stopping point while the trace is stored in real-time and saved for review. A deep trace gives the designer the information necessary to capture the source of the problem, but not the ability to filter the data. What he or she wants to do is reduce the data, or filter it by searching for a complex series of events. Even when working with a small portion of the code, say 10,000 lines, in a multitasking system such as a tape drive, the designer may have to sift through millions of cycles to locate a problem. Not only do you have to determine if the event desired is in the large trace, you have to find it. One way to deal with this is to prefilter what goes into the trace. The power of a logic analyzer is in not only what it captures but in what it can discard.

SAVING TIME

The designer should try to save only the area of interest. This conserves not only trace memory but the designer's time in sorting through it. For example, after the real-time kernel is debugged, there is usually no reason for it to go into the trace. Here's where the hardware storage qualification in the analyzer becomes important. By arranging links to put all such system code together in a contiguous memory, a single "do not store this range of addresses" trigger specification will keep it out of the final trace as well as show how much time such overhead consumed. The designer can also set up to store other singular events such as a "read from hardware memory locations" or "fetches from specific routines." This reduces the memory requirement needed to associate separate events in time *(Fig. 4)*.

Another way to track down problems captured in the trace is to apply various levels of analysis to the same data. For example, by looking at the trace at the hardware level, all activity on the bus is revealed. This includes interrupts and direct memory access (DMA) cycles. Filtering the data, allowing only executed instructions to be displayed, is valuable when tracing detailed software execution. Further filtering, displaying only subroutine or branch flow, allows a higher level analysis of the overall program flow.

The combination of these tools can quickly isolate a wide variety of problems, the sources of which are not apparent from the observed fault. The



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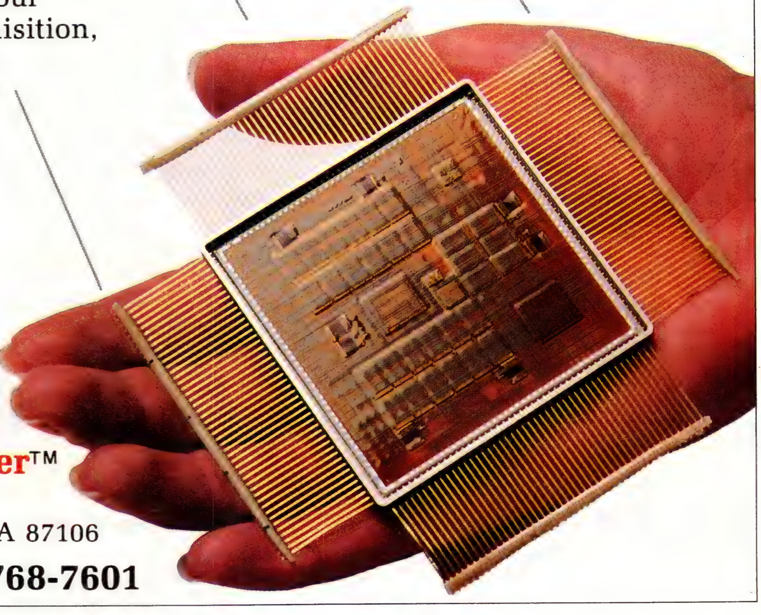

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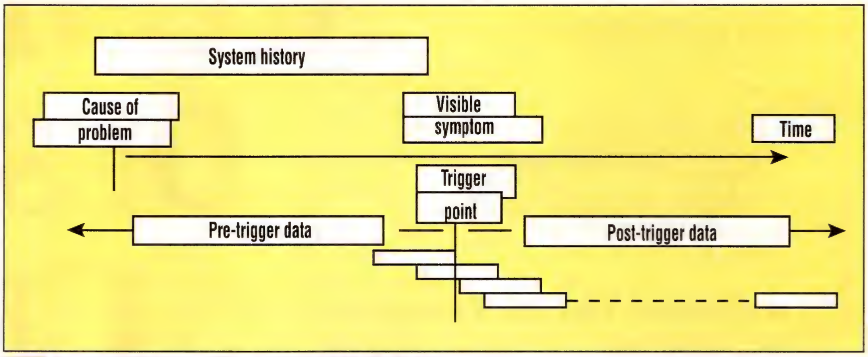


3. DEEPER TRACE MEMORY is required to isolate system faults that can take minutes to exhibit themselves. You can't acquire this data without deeper memory.

combination also helps later in the development cycle, when optimizing code. By using the system analyzer to time specific portions of code, the designer can verify the time required to execute certain routines, such as interrupt service routines. One can take this even further and monitor multiple functions to find out the time spent in each routine, relative to the whole program. This lets the designer identify places within the code that, if optimized, will significantly improve the performance of your whole system.

INTEGRATION

Hardware/software integration problems are often more difficult to debug than program logic. They require physically monitoring the target system. Using hardware tools to correlate specific signals with instructions, the designer can debug complex problems such as why a certain series of instructions cause hardware errors or why a specific data pattern causes glitches on the data bus. Here is where the designer also sees system-level race conditions. This is helpful when several parts of a system signal an error and the designer has to resolve which one signaled it first and the appropriate priority.

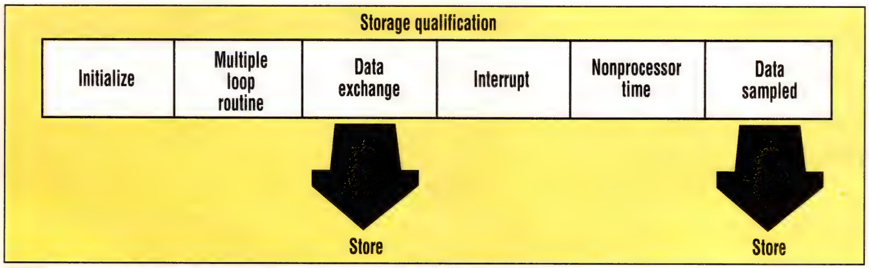
For example, repositioning the tape for a retry following a read or write error sometimes can be done by the servo subsystems; other times it may require rereads of previous blocks. Proper tape positioning is critical in maintaining the integrity of the data, but it can be difficult to verify. It is one of the most important integration tasks. Even a small amount of physical tape mispositioning can result in overwritten or duplicated data records.

The state-oriented trigger machine of the logic analyzer is used to trace the sequence of hardware/software events to isolate the fault. Records on tape are separated by interblock gaps, or IBGs. Since the drive must accelerate the tape to speed before read or write data can be clocked, the physical position of the tape at rest can be difficult to correlate to its logical position with respect to data blocks. This becomes a nasty problem to verify on the fly. It is one of the biggest problems of error recovery operations with regard to the real-time integration.

With the CY611 processor, everything is internal to the registers. If one subroutine returns a code that indicates a failure, the only way to find what branch it took is to see a failure code. A way around this real-time register blind spot is to include a debugging macro that writes to an unused "write-only" location. Any time the main function that evokes error recovery is called, for example, this macro writes an integer value representing the register contents to the write-only location.

The logic analyzer reads this value off the bus and into the trace buffer. In this way, the designer can see error codes, fault symptom codes, error classes, and block IDs, which might otherwise be inconvenient or impossible to examine. Such a macro is often included via a conditional compile and may also be used as a method of providing a ready trigger spot on unusual failures or on branches that execute only when there is a failure.

This write-only technique does affect timing by adding a write cycle but is generally not intrusive to any other part of the target system. Earlier in the design phase, the designer can use the debugger to run diagnostics. When the development is far enough along, the tape drive can be interfaced to a host system. This is where a logic analyzer is particularly useful—its non-intrusiveness makes it possible to see how the system actually runs at full speed.



4. TRACE MEMORY IS SIGNIFICANTLY extended by using real-time storage qualification to capture only the data of interest.

UNATTENDED TESTING

Long-term test can be set up to run hundreds or thousands of passes unattended. Running the same tests used by the quality control department earlier in the development cycle reduces the total design cycle time and provides a time-effective method of duplicating failures to provide additional debugging information.

Finally, when fixes are implemented, the system analyzer can be used to verify that the tests execute them as anticipated. Often there are times when the power of both the debugger and the system analyzer are needed at the same breakpoint. The general example is when the system must run in real time up to the breakpoint with the execution stream stored in the trace buffer. The debugger must simultaneously regain control at that point for further analysis.

When XRAY sets a breakpoint, the designer wants the analyzer to trigger the second time the debugger executes a routine. This is because the debugger copies a block of code over

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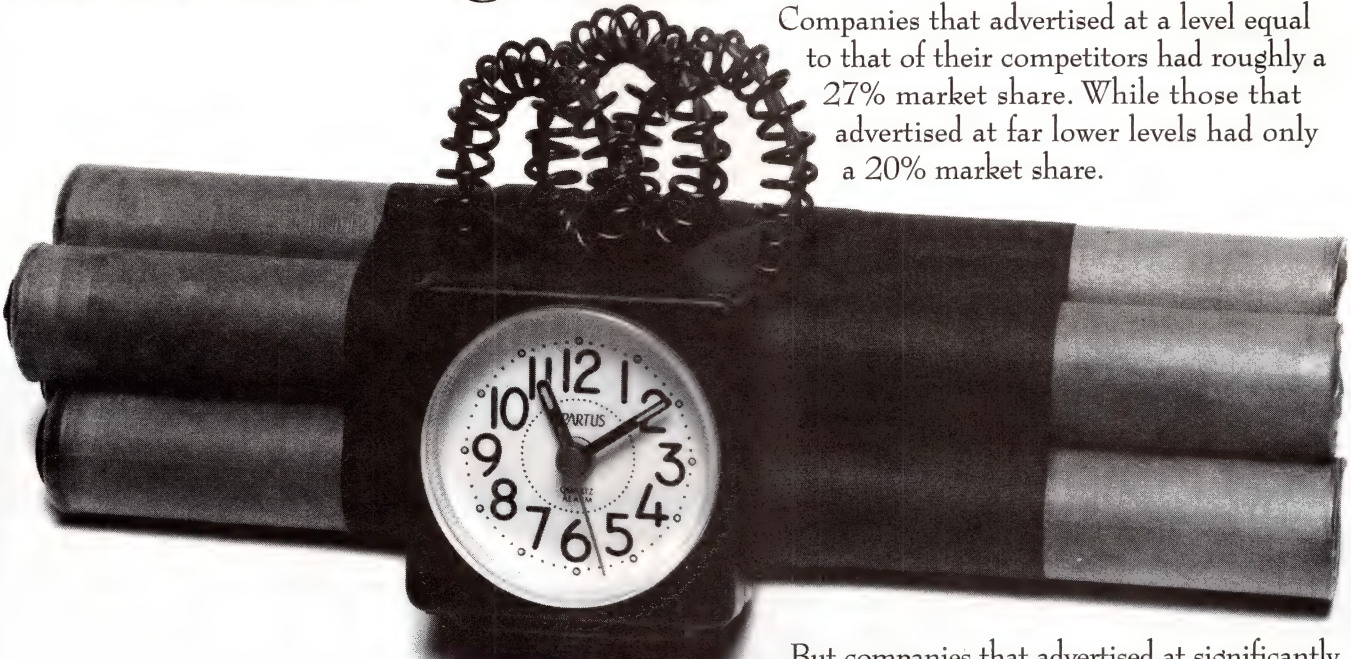

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to scratch-pad memory and patches it in. To deal with this, a specific trigger was built for the logic analyzer to execute on the second debugger breakpoint. With this, the designer can use the debugger to control the triggering process, but with only a single generic trigger, and without having to update the logic analyzer repeatedly.

CROSS-COMPARE DATA

The workstation-based X Windows system helps the designer to do much of this cross-comparison of data. One can have, at a single workstation, several different windows displayed simultaneously. These windows include: command tool, editor, debugger, listing file, written scripts, symbols, and the DAS. The designer can print screens, transfer trace memory from the DAS to the workstation, and do some limited cut and paste between applications to correlate data. When working on a particular fault symptom code, for example, the designer can look it up, see a system trace on the DAS, examine memory with XRAY, and run scripts s/he has created to provide other information about symbols, the link map, and so on.

Having both software and hardware tool displays on the screen makes analysis easier. By extracting the symbols from the compiler and routinely downloading them over the LAN to the analyzer, the analyzer can display higher level information such as routine names and reference back to the source code. The designer can also use remote batch instrument control to load test set-ups or save traces. This improves on trying to transfer a 10-Mbyte trace on floppies, once the only solution.

Embedded system debugging takes advantage of the data correlation benefits offered by enterprise instrumentation. When a system integrator can view different windows on the same screen that show target processor activities, software source code, assembly code, performance analysis, and the debugger, both integration and debugging can be performed faster. When designers can access all the tools they need from their workstation and when they can see various levels of data analysis at one time and have access to non-intrusive system analyzers for the real-time and hardware/software integration components of the development process, they will be able to do their jobs more efficiently. Their companies will also be able to maximize their equipment budget to the benefit of the entire design team. ☐

Mark Call is a senior development engineer at Storage Technology Corp. He has been both a hardware and a software designer and has real-time development expertise in tape drives, optical drives, and high-end printers.

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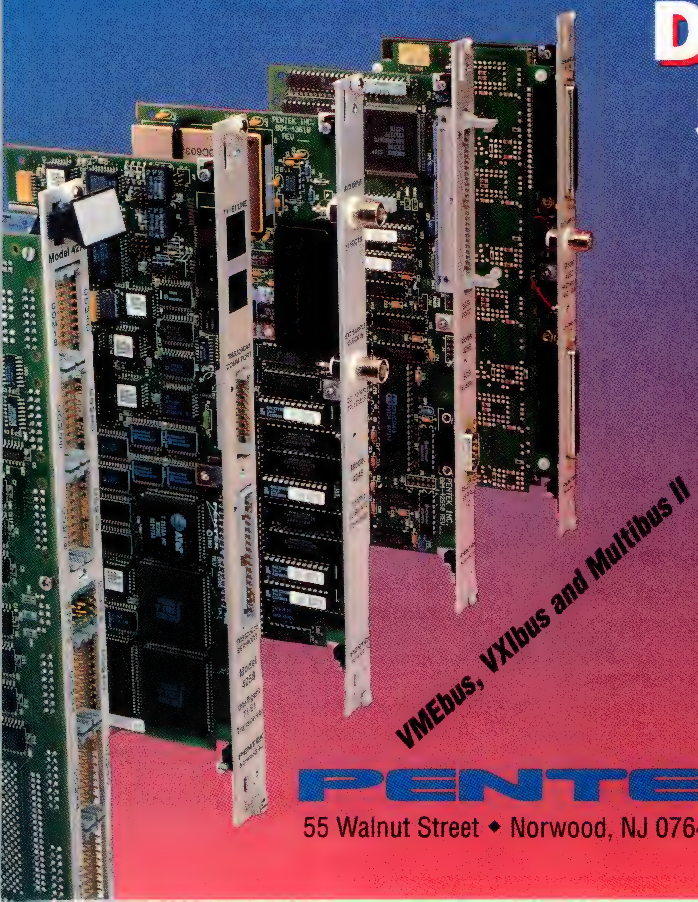

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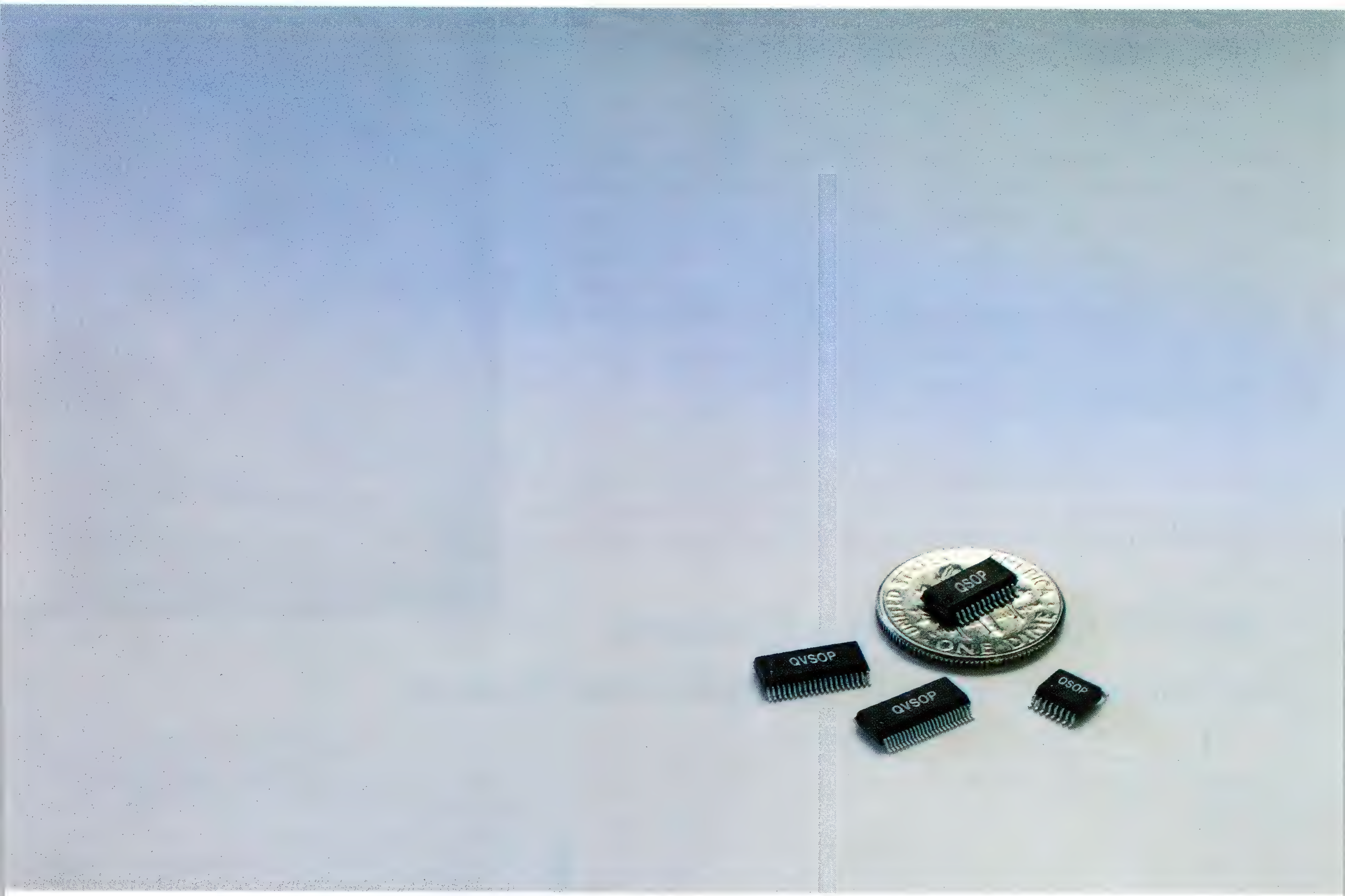

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Design Engineering Bulletin

New Product and Applications Information for Design Engineers

X88C75 SLIC® E^2 Microcontroller Peripheral adds I/O ports, E^{2}PROM, Static RAM, Interrupt controller and Address Decoding Logic to 80C31 Family

The X88C75 SLIC Microcontroller Peripheral is the ideal enhancement to 80C31 type systems. The device features 8K Bytes of E^{2}PROM which may be used for either program or data storage and 16 bytes of static RAM for data parameter storage. The sophisticated 16 I/O lines are configurable as either Inputs or Outputs with two additional strobing signals for either latching data into the ports or for strobing data out. The Programmable Interrupt controller can be configured to generate interrupts from either data input into the ports or the completion of the internal E^{2}PROM write cycle. The E^{2}PROM features concurrent read during write operation which allows the controller to continue program execution from the E^{2}PROM during a write cycle to the same device.

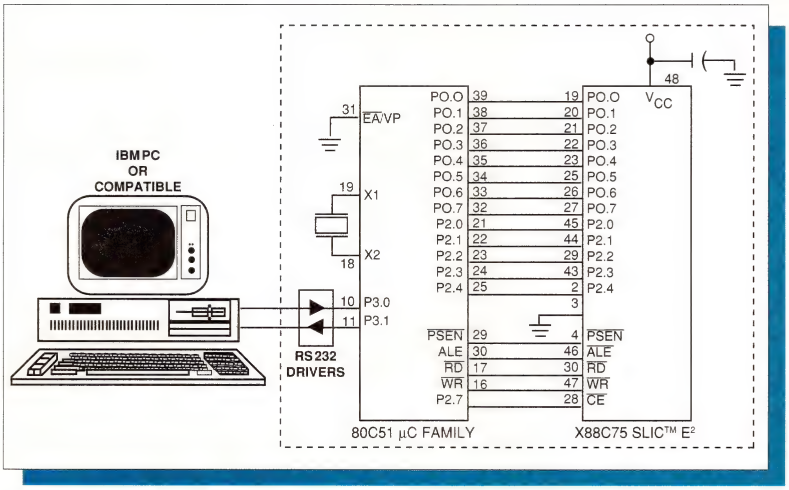
All internal resources are memory mapped and their location is programmable through the internal nonvolatile programmable decoder. This allows multiple X88C75 SLIC devices to be used to provide up to 64K bytes of E^{2}PROM, 128 Bytes of RAM and 128 I/O lines without any additional logic. The X88C75 SLIC device also features an optional LAM (Latched Address Mode) mode of operation where the 8- I/O lines of port B are used to output the de-multiplexed low order address byte of the 80C31 bus. This simplifies the inclusion of standard byte-wide memory devices such as SRAM, NOVRAM or EPROM into the system applications.

X88C75 Combines E^{2}PROM, RAM, I/O Ports and Interface logic into an integrated, cost effective E^2 Microperipheral.

X88C75 SLIC Provides Complete Solution to Firmware in Embedded Systems

The need for software upgradability is becoming increasingly important in embedded systems. The X88C75 SLIC device provides a complete hardware and software solution to this need. The device is delivered with a small library of routines loaded into the device. Upon initial power-up, the 80C31 will be initialized, and the SLIC firmware will download the applications software through the UART on the 80C31. Subsequent downloads can be performed by re-invoking the SLIC firmware to allow the applications software to be changed once the system is in the field. The software update can be performed over an RS232 interface, a network connection, a local serial bus, RF link or a fiber optics cable. The updates may be performed in a random fashion allowing a single byte, numerous bytes or the entire applications program to be updated.

Designing systems based on the X88C75 SLIC E^2 is simplified by making the SLIC firmware routines readily available to the application software. A PC based program called XSLIC was developed to handle the X88C75 SLIC to host system interface. The XSLIC facilitates reconfiguration of the communication link parameters and downloading application programs to the target system. Provisions have also been made to relocate the SLIC firmware in case of address conflicts with on chip resources of the 80C51 derivative employed by the system.



Upon initial power-up, the 80C31 will be initialized, and the SLIC firmware will download the applications software through the UART on the 80C31.

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DEBUGGING FOR REAL TIME: HARD CHOICES

BECAUSE EVERY TOOL HAS AN EFFECT ON THE SYSTEM, KNOWING YOUR TOOLS IS THE BEST DEFENSE

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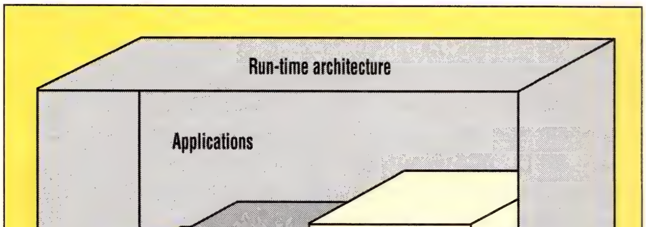
Has your favorite debugger ever broken the system by its simple presence? That happened because every tool has some effect on the system, and real-time systems, with their deterministic requirements, are very sensitive to intruders. Knowing which tool to use and what its effect will be on the system is vital. In this article, we will explore the range of available tools and see their strengths and weaknesses. Just as a good carpenter should know his tools, note that the programmer's tool set includes source-code debuggers, regression tests, system profilers, and firmware debuggers. Development environments offering a rich and varied set of tools gives the best advantage to finishing a project on schedule and within budget.

These high-level debuggers display the source code of a given task, process, or low-level routine and simultaneously control the execution of the target hardware. With the ability to set break-points in source code, examine and modify variables, and even profile execution of the code to locate "hot spots" in need of optimization, these debuggers prove their worth daily.

The "tbx" debugger in Unix System V Release 4 is one such tool. Integrated with the VMEexec real-time development system from Motorola Computer Group *(see the figure)*, this X-Windows-based program offers the features expected in a mouse- and keyboard-savvy implementation for debugging real-time tasks, drivers, and system software across multiple processor boards, each of which is running the pSOS+ real-time kernel.

Even a multitalented tool has its limits—source-level debuggers need sophisticated display terminals. X-Windows display devices need high-bandwidth Ethernet communications and they place a heavy, non-deterministic load on the supporting system. Even when the "target" is different from the system supporting the display, the high intelligence of the debugger requires a lot of information from the target processor, and supplying that information is overhead—overhead that modifies the behavior of the target. More than once, I have tried to use one of these debuggers to help find a problem only to see the problem disappear when the debugger is present, and reappear when it is removed.



THE VMEexec RUNTIME architecture supplies various interface layers to allow application developers to choose the most appropriate layer for the task. Real-time applications have several interface points to acquire their services: through Xll libraries (Xlib); through SVIDlib or NETlib; directly to pSOS+; directly to an I/O driver; or directly to the hardware.

At the low end of the test-tool spectrum is the firmware-based debugging monitor. These rarely have more than very limited discourse with the user, and then only with a narrow set of commands and options. But with their quiet "sit in the back of the room until called" attitude, the firmware debuggers often cause the least amount of upset to a real-time system. Although difficult to use and hard to interpret, this class of debugging program is often the back up position in contemporary systems. In the field we may not be able to fire up the sophisticated Unix-based development environment with our source files, X-Windows debugger, and support tools, but when all else fails, the lowly firmware debugger is still there. Developers who can profit in this bleak but unobtrusive environment will obviously stand a better chance of fixing bugs.

Most board vendors offer firmware with their products. And as the basic hardware on the boards changes from one design to the next, it is important to offer the developer a basic set of commands that is consistent across all models. Vendors with a wide variety of offerings have the same problems that developers do and they attempt to keep the firmware differences, as seen by the users, to a minimum. A vendor with a wide product offering with similar firmware on each model ranks high on many engineers' lists.

OS-SPECIFIC TOOLS

In between the firmware and source-level debuggers and sometimes partially integrated with each of them, are the OS-specific tools, such as pROBE+ from Integrated Systems Inc., which is incorporated in the VMEexec development tool set. These programs display information about the software objects within the system. These tools tell the programmer which tasks are ready to execute and which are not and why. OS-specific debuggers display system resources and allow the engineer to monitor activity within the system. When a deadlock or runaway condition occurs, the debugger supplies the precise view needed to see what went wrong.

Of course, counting events takes time and in a finely tuned system, this may be just enough to mess up the works. Worse still, turning the performance gathering software on and off may induce new glitches or hide old ones.

Many times the best tool is one created by the programmer—to watch for a specific set of conditions or to help characterize an obscure problem. Often, this tool is the simple "printf" (or other print-like) statement.

"I can't debug without printf," has been uttered by many productive engineers. A custom-crafted tool placed at a strategic point and displaying critical chunks of information may be exactly what is needed to get the proper insight.

Sometimes it is appropriate to output this data onto a serial port where the engineers can watch what is happening in real time. Or they want to redirect the output into files for later examination. In VMEexec, the standard output data stream from tasks can be redirected into a file on the target processor or even into a file on the development system. This latter capability, used with the reassignment of the input stream to a set of test data, is very useful for regression testing of application software in real-time systems. Reassignment in VMEexec is handled in a simple environment file containing one line of text per data stream.

```
STDIN=/host/usr/edski/testdata/case0042.in
STDOUT=/host/usr/edski/testdata/case0042.out
STDERR=/host/usr/edski/testdata/case0042.err
```

These three lines connect a real-time task's input and two outputs to the specified files on the host file system, the Unix system from which the tasks are downloaded into the real-time processors.

Reassignment with host files offers an enormous boost when faced with a complex system to test. But as with the other tools, there is a performance penalty: Not only is there additional overhead in moving data between Unix and the real-time processes, but there is also the danger of an inadvertent infection of the Unix system's non-determinism into the real-time system. As with the other performance effects, this too may create artificial and false bugs.

Ultimately, any tool may create new problems. The trick is in deciding which tool to use when, and in knowing how it will affect the system.

Testing begins at a module level when a programmer creates a set of test data to pass through a routine to verify the output. As the testing progresses, the programmer adds more test cases and expands the software with more code, more routines, and more possible scenarios or combinations. Much of the trick of adding more software at this point is in not breaking what is already working. Hence the need for regression tests.

Regression tests verify that what worked yesterday still works today. These tests grow throughout the life of the project and eventually become the meat and potatoes of the final tests.

But as module testing progresses and more routines are integrated, the level of detail provided by a simple printf becomes more of an avalanche of information. Engineers must begin reducing the amount of raw output by streamlining the test cases.

Large portions of the system may be falling into place by this time. Tools presenting the interactions of modules more than their individual contents are often more valuable. OS-specific tools, which display tasks, messages, semaphores, and other OS-type objects, may prove more useful in these intermediate stages of integration. When all the pieces are in place, tools that present the broadest view may be helpful, but only when their measurements are possible with infinitesimal perturbations to the system's performance. Finally, all the tools have to be removed and only the regression test suite or real-life can be used to ensure correct operation; eventually someone must take it out for a test drive. When problems develop, engineers modify one piece, test it, and reassemble everything and run it around the track again. Each of the foregoing tools is pulled out of the toolbox as needed and tossed aside while the next test is run. A tool's ability to be inserted and then removed quickly may be one of its greatest virtues. A rich and varied tool set with the ability to give several different views of the system is essential in today's complex systems. ☐

Ed Skinner, an instructor and software developer for Motorola's Computer Group, has designed and programmed real-time systems for 25 years, can be contacted by e-mail: edski@phx.mcd.mot.com.

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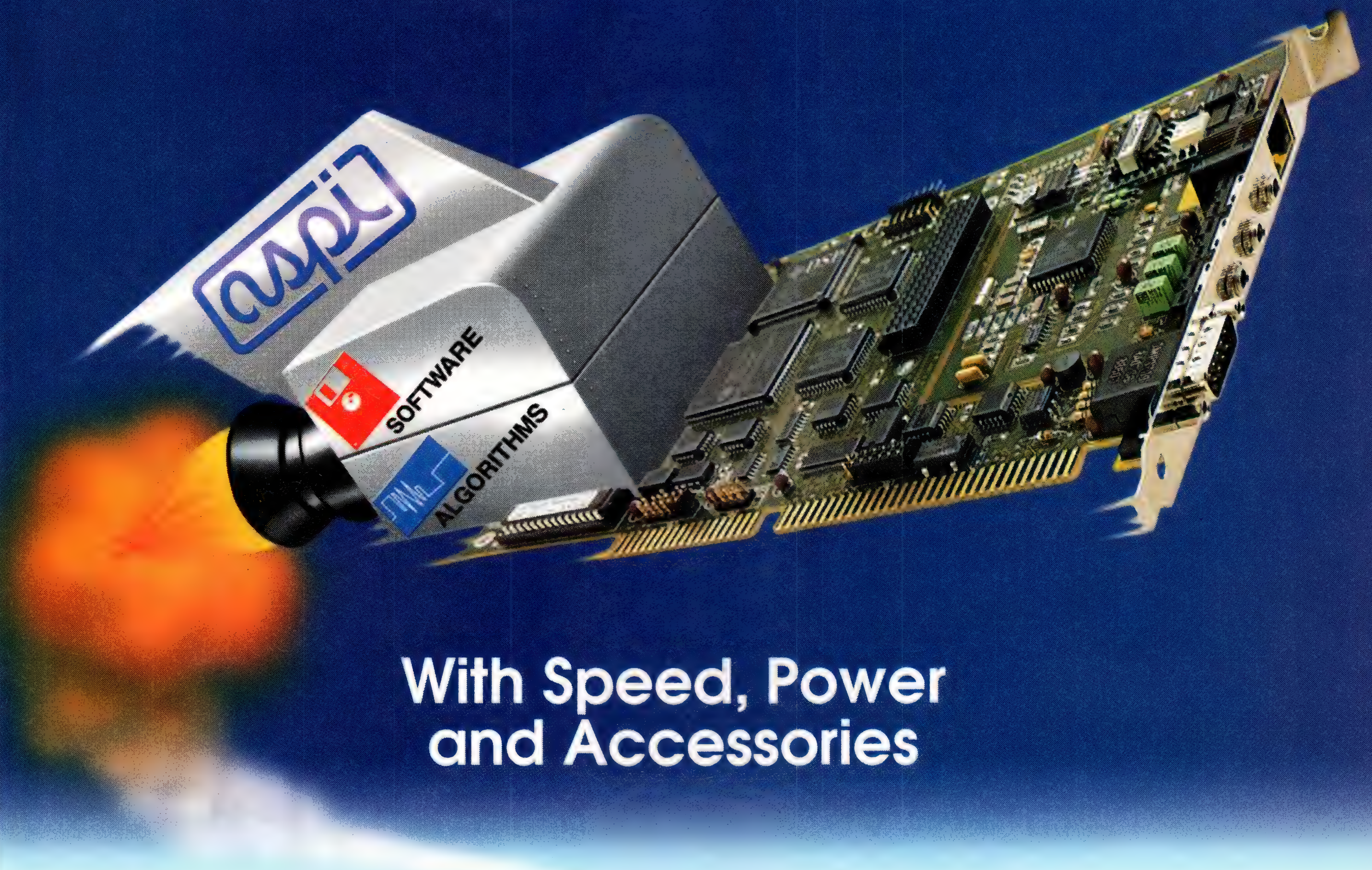

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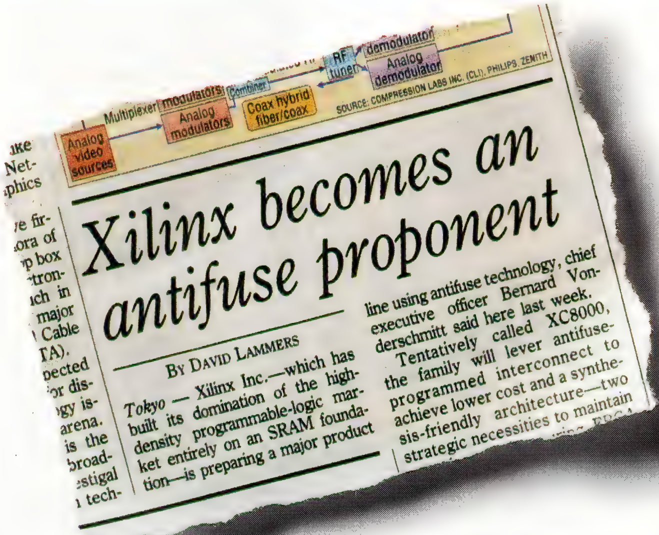
We couldn't have said it better ourselves.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Xilinx becomes an antifuse proponent

By David Lammers

Tokyo — Xilinx Inc.—which has built its domination of the high-density programmable-logic market entirely on an SRAM foundation—is preparing a major product line using antifuse technology, chief executive officer Bernard Vonderschmitt said here last week.

Tentatively called XC8000, the family will lever antifuse-programmed interconnect to achieve lower cost and a synthesis-friendly architecture—two strategic necessities to maintain

Electronic Engineering Times, May 23, 1994

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ELECTRONIC DESIGN QUICK LOOK

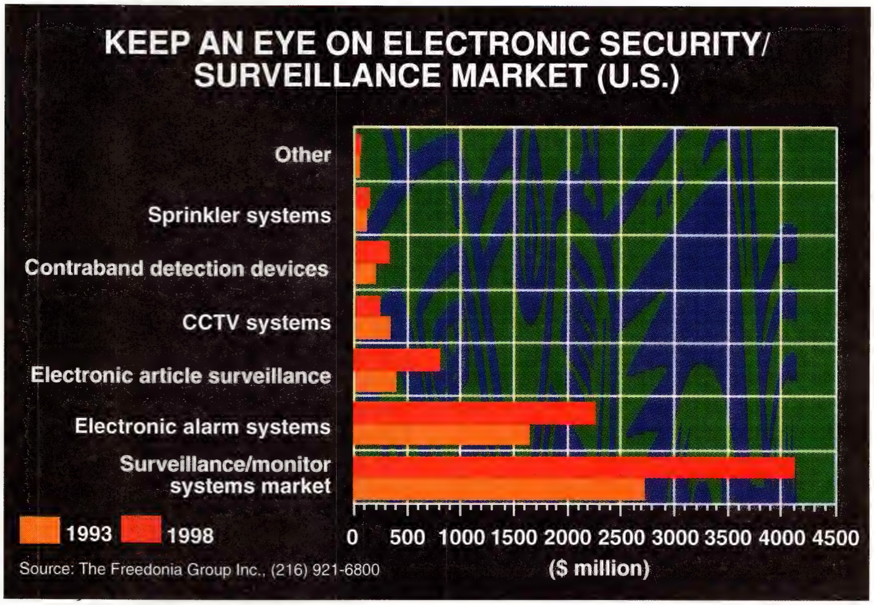
EDITED BY SHERRIE VAN TYLE

MARKET FACTS

The market for private security surveillance and monitoring systems is expected to increase 8.6% a year through 1998, to be worth more than $4 billion that year, according to a new study by The Freedonia Group, a market research company based in Cleveland, Ohio. Influencing growth are innovations in sensors, improvements in signal transmission, and increasing miniaturization, say the researchers.

Among the product categories, electronic article surveillance (EAS) systems and contraband detection devices (such as bomb and metal detectors) show strong growth prospects. The EAS systems are making inroads in the relatively untouched retail sector. Demand for contraband detection is increasing for industrial and commercial sites as well as in airports and school systems.

Closed-circuit TV (CCTV) and central station alarm monitoring systems also have above-average prospects for growth, say the researchers. CCTV will take advantage of such innovations as time-lapse recording, night vision technology, and increasing miniaturization of systems.



KEEP AN EYE ON ELECTRONIC SECURITY/ SURVEILLANCE MARKET (U.S.)

Source: The Freedonia Group Inc., (216) 921-6800

TALES FROM A SKUNK WORKS

Who causes the problems in industrial age companies? "They" do, those "other people." Slash and burn era bureaucrats thrive on rules, conflict, accusation, and fear. Bureaucrats follow procedure and push problems over the horizon to another part of the enterprise. Those on the other side of the horizon, of course, do the same. The old ways are blame-based, internally focused, and problem-centric.

It is better to target results and opportunity. The trick is blending "us" and "them" into a team where one plus one equals ten. A skunk works often can do that. The old ways allowed taking advantage or exploiting power if the rules were followed. However, selfish or controlling behavior destroys high-impact teams and cannot be allowed. From "neutron Jack" Welch at General Electric to analytical Gil Amelio at National Semiconductor, leading CEOs are learning they must cast out even productive employees and managers who can't adapt to the new systems. People who play win-lose games undermine high-effectiveness organizations.

U. S. business is unprepared for teams. Outside sports, many people are afraid to rely on teammates. Our society customarily allows "legal" but unethical behavior. This must stop. Cheaters must be isolated or banished for the new organizational paradigms to flourish.

The contest in the future is between selfish, individualistic capitalism (our way), and team-based collaborative capitalism (the Pacific Rim way). These are very different philosophies. Since it takes teams to do products, the latter model is winning.

We are still learning how to best lead and reward teams of knowledge workers—the old model, where the boss knows best, is hopeless. Autocratic decision-making processes do not work well in subtle, uncertain, or chaotic environments. From Eastern Europe to mainframes, centralized processing is outmoded.

You use teams like skunk works for breakthrough performance gains. But if some in your firm are pursuing hidden agendas, you might get worse results than from the old ways. Team members should know more than their leaders about the task at hand. Why not tap this knowledge? When teaching graduate students, I use both individual and team grading. Team members rate the contributions of their peers, and the class gets to judge me and the course. Moving to the new information-age business methods takes work, investment, and training. You need leaders and coaches. First you need a sponsor, funding, and an empowered team leader. Only then can you start team building. The proper techniques are shared vision and accountability, not process and control.

John D. Trudel, CMC, is managing director of The Trudel Group, 52001 Columbia River Hwy., Scappoose, OR 97056; (503) 640-5599.

QUICK NEWS: SEMINARS

Engineers grappling with circuit, packaging, and system design may benefit from a tutorial and training course given by OptEM Engineering, a supplier of interconnect-analysis tools. In the two-day program, engineers train with design-automation software that analyzes signal integrity, ground bounce, and crosstalk problems. Day one includes electromagnetic-field theory and modeling, transmission-line theory, and modeling of complex 3D interconnect. The second day covers Spice transient analysis, crosstalk prediction, radiation patterns, and interconnect design under strict EMC requirements. The course will be held in San Jose, Calif., Sept. 20–21 and Dec. 6–7. Cost is $1500 per attendee. All participants receive a free 30-day evaluation of the OptEM software. For more information, contact course-leader Dr. Juliusz Poltz at OptEM Engineering Inc., 100 Discovery Place One, 3553-31 St. N.W., Calgary, Canada T2L 2K7; (403) 289-0499, fax (403) 282-1238. *LM* CIRCLE 460

OFFERS YOU CAN'T REFUSE

Hardware designers, software engineers, and hardware/software integration engineers working with embedded systems may be interested in attending Hewlett-Packard's 1994 Embedded Mini Symposium. The free sessions will be held in various U. S. cities beginning in early September (for example, in Houston, Sept. 12; Orlando, Fla., Sept. 16; Rockville, Md., Sept. 22; Piscataway, N.J., Sept. 26; and Burlington, Mass., Sept. 28). Hardware and software tracks will cover case studies focused on system integration, root-cause debugging of complex systems, real-time considerations, optimized design techniques, and software development productivity techniques. Attendees receive a copy of the technical presentations. To register, call (800) 765-9200.

A CD-ROM disk demonstrates the WindView graphical analysis tool for embedded-system development. With WindView, a designer can visualize the complex interaction among tasks, interrupt service routines (ISRs), and system objects within an application. The free CD ROM runs on a Sun workstation. For a copy of the disk, contact Wind River Systems, 1010 Atlantic Ave., Alameda, CA 94501; (800) 545-9463. CIRCLE 461

KMET'S KORNER

...Perspectives on Time-to-Market

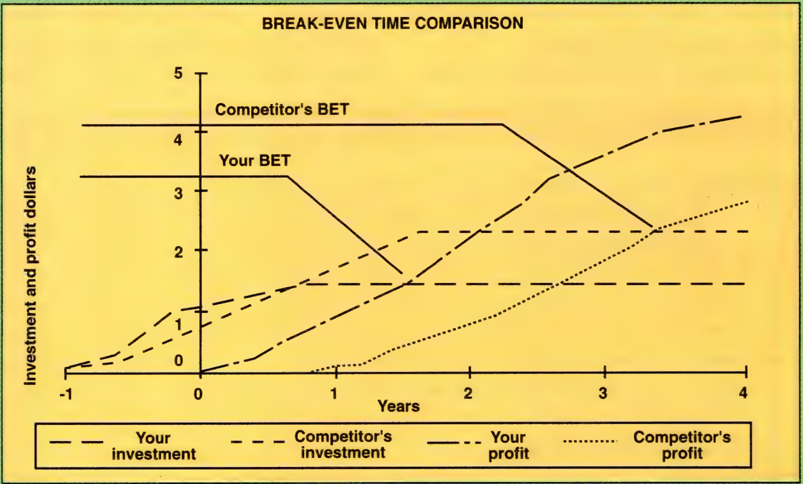
BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 1070, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804

A break-even time (BET) chart on a new product, while useful, is easily forgotten. Two dominant reasons contribute to the effect: one, the time between the production of the initial chart and actually breaking even can be rather long; and, two, if the time between forecast and actual becomes too drawn out, accuracy is compromised.

Conventional BET presentations plot investment and profit forecasts as the reference. With the passage of time, actuals get recorded on the chart. On the fastest of programs, the x-axis calibration ranges from 12 to 24 months from staffing start to actually breaking even. On more complex, or lightly staffed jobs, times extend by factors of 2, 3, or 4—years can go by between the time of the initial forecast to the production of actual investment and profit numbers. Now, judge the usefulness of a BET chart on an effort that takes 3 years to get to market and then another 3 years to break-even. Or what would you think about a chart showing two years of investment and then one more year to break even, for a total of three years?

As the length of the x-axis expands, chart believability contracts. It's just not possible to make an accurate investment and profit forecast that looks four, five, or more years into the future. And if someone thinks they can make one, who believes them?

So what do you do to extract maximum benefit from the break-even time concept? First, you need to get the x-axis calibration right and then you have to make it believable. To do it, add information about the competition to your BET chart *(see the figure)*.



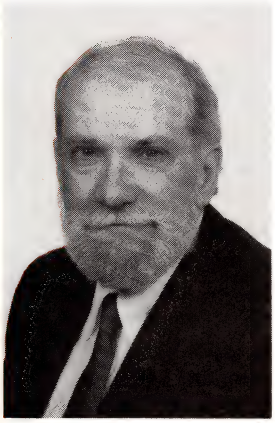
Placing competitive information on the chart when it's first generated forces the production of realistic, time-based decisions. If your competition takes 9 months to get product to market and breaks even in another 9 months, you know what you have to do. And if they take three years to get to market and consume another three years in the market to break-even, you still know what you'll have to do. Addition of competitive goals gives the BET chart true meaning—the more competitive the challenge presented, the more meaning!

Ron Kmetovicz's The One-Minute Time to Market Self Assessment, which identifies five key behavioral patterns exhibited by fast-moving new product development organizations, is available free to the readers of Electronic Design by contacting Time to Market at the address above.

...Tree huggers and old geezers

BY FRANK J. BURGE

Director of Market Development for Electronic Design



Some months back I used the phrase *tree hugger* to describe managers who won't let go of the old ways, even though the old ways may not make it in today's competitive market environment. My choice of tree hugger brought a response from a number of folks who live in the West. My friend Art Heller pointed out that in his town, calling someone a tree hugger is a preliminary to a "helluva fight." He lives among people who are often violently divided on environmental issues—those who make their living in the lumbering industry and those who think the industry should be tightly controlled to preserve a livable environment.

Art observed that those supporting the environmentalist position are variously known as tree huggers, enviros, greens, or just plain SOBs. While those supporting the lumbering industry or developers are generally called rednecks, Neanderthals, or Wahoos. And in another recent column, where I talked about the generational wars, I talked about old geezers. Art, who runs a marketing company with its headquarters in Placerville, Calif. in the Sierras, once again took me to task.

Mostly, he thought my reminiscences of life and work in the good old days emphasize that I've gotten old, or worse, that I'm feeling old; maybe I've even become one of those old geezers. Nine years my senior, Art threatened to come down from the mountain and kick my butt if I keep it up. He suggests that as we get older, we should curb our tendencies toward reminiscences, keep ourselves in reasonable repair, and get on with life, taking full advantage of the experience we have gained to date.

Another comment comes from an "older" member of the marketing community, who suggests that the younger crowd, at least in marketing, is better trained and better informed on the theory and mechanics of marketing than we were when we started out. But, at the same time, they are naively dedicated to statistical analysis of the unmeasurable and the objectification of the subjective. As a result, they analyze everything to death, wasting precious time, to say nothing of the dollars thrown down the drain. In many companies, the old-fashioned gut feeling, a product of experience and market savvy, has been replaced by analysis paralysis.

He concludes by observing that the younger crowd would never really understand why *Death of a Salesman* might bring tears to our eyes. The final pearls of wisdom on the generational wars come from my barber, who is one smart cookie. After 50 years on his feet, he's working four days a week; he takes Friday, Saturday, and Sunday off and works evenings the rest of the week as a convenience for his old-time customers, He's taken on a younger barber as a partner, a recent graduate of the Molar Barber College, with a post-graduate degree in hair nutrition. When I asked my barber for his opinion on the generational wars, he dismissed the entire notion with an expletive deleted. He sees it as a natural passing of the mantle from generation to generation, just as his grandfather passed the clippers to his father and he to his three sons. And my tonsorial wizard thinks the younger barbers are better trained, know more about hair therapy, and can stand longer without their legs cramping. But since my barber knows more about life and is a far better storyteller, for their $9, his customers get more than a haircut.

Digital Signal Processing

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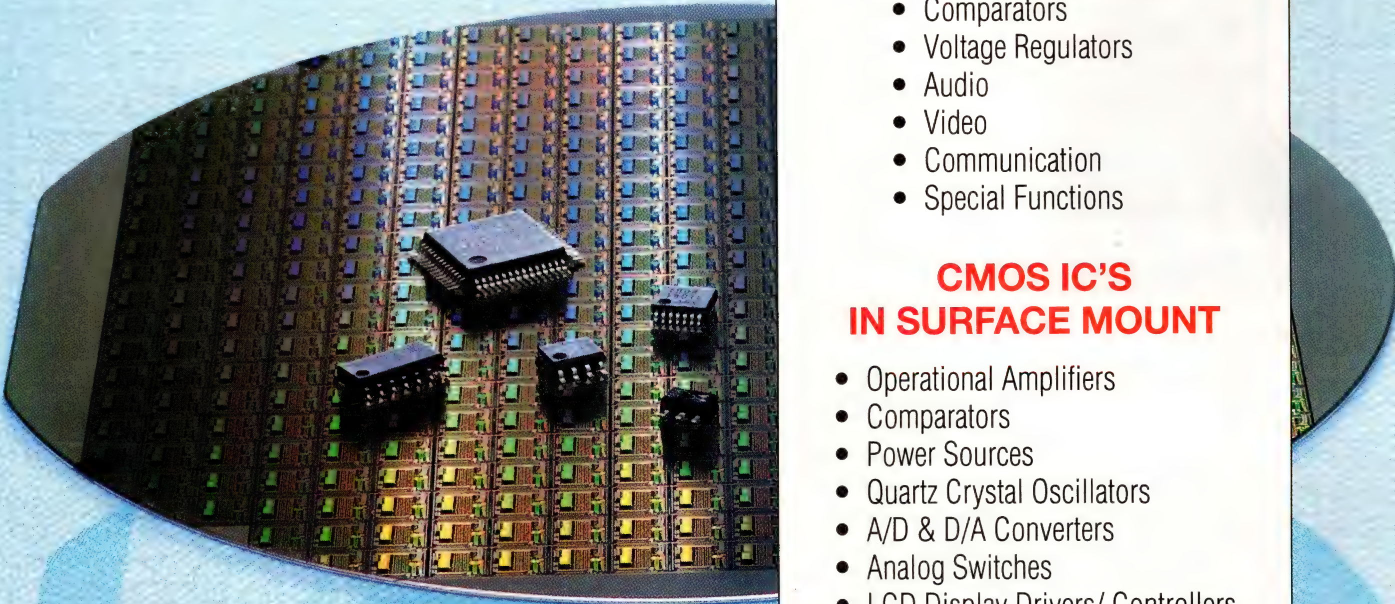

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READER SERVICE 163

CIRCLE 520

COMPARE VCO, INPUT FREQUENCIES

W. DIJKSTRA
Oude Kerkstraat 14, 5581 JH Waalre, The Netherlands.

Comparison of an input signal's frequency (f_i) with that of a voltage-controlled oscillator (f_{vco}) can be accomplished with just one CMOS phase-locked loop IC and a transistor *(Fig. 1)*. The phase and the frequency can be compared with a phase comparator, which, along with the VCO, is part of the HEF4046 PLL IC. The transistor helps introduce hysteresis, enabling the circuit to be used as a switch driver. One possible application is a low-light sensor that turns on lights at twilight.

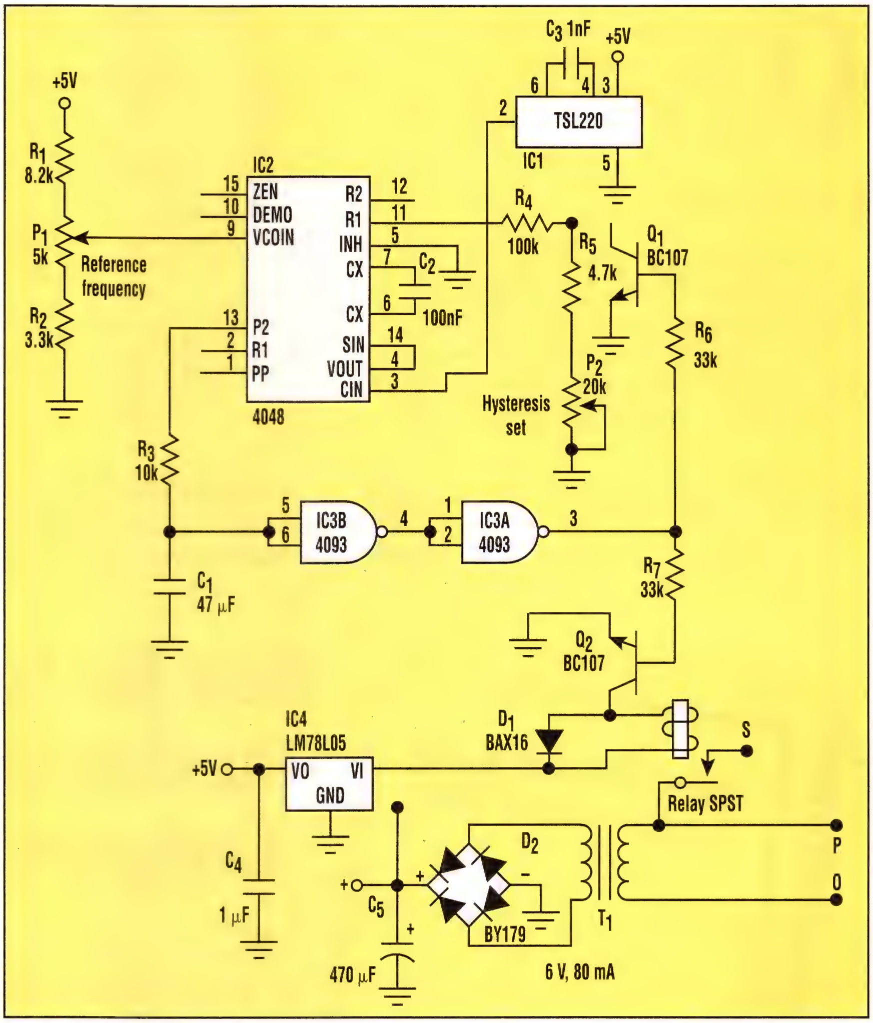
In the circuit, when the input frequency, f_i, is higher than f_{vco}, the output signal from pin 13 (phase comparator output II) is low, and vice versa—the output goes high when f_{vco} is higher than f_i. In the second case, with a high output, the transistor conducts so that resistor R_2 is short-circuited and f_{vco} increases further by an amount determined by the resistance ratio $R_2/(R_1 + R_2)$. This extra frequency increase determines the hysteresis.

The circuit in Fig. 2 offers one practical application of the circuit, namely a twilight switch. The light detector is a TSL220, a light-to-frequency converter developed by Texas Instruments. As its light input decreases, its output frequency decreases. When the TSL220's output frequency falls below that of the VCO, the circuit triggers and turns on the relay.

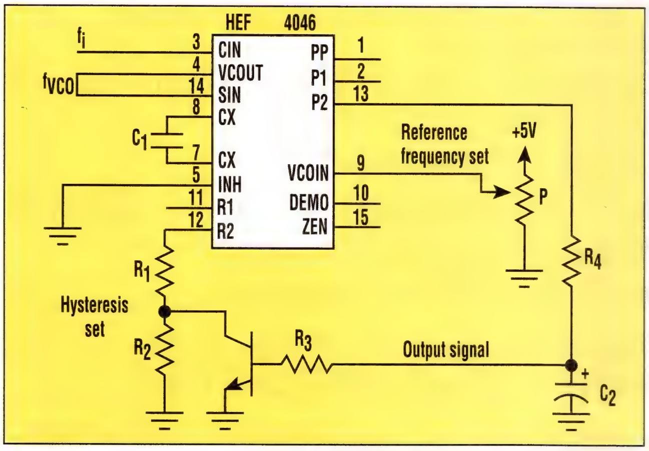
In this design, the detector's output frequency varies from 5 Hz to several kilohertz, depending on the amount of incident light.

The VCO's frequency is set with the reference potentiometer, and its range is limited from 2 Hz to 200 Hz to match that of the TSL220 during twilight.

The R_3-C_1 combination causes a delay to avoid effects of stray light sources, such as passing motor cars. However, it requires the use of two Schmitt-trigger NANDs to prevent relay chatter. (Note that Texas Instruments suggests the use of a grounded guard ring around pins 6, 7, and 8 as well as the capacitor leads, to isolate this input from potential leakage currents.)☐



2. A TWILIGHT SWITCH can be created using the circuit in Fig. 1. The light detector is Texas Instruments' TSL220 light-frequency converter.



1. JUST one CMOS IC and a transistor are needed to compare an external input signal's frequency with the frequency of the signal from a voltage-controlled oscillator.

CIRCLE 521

CONVERT TO DIGITAL FILTERS WITH EASE

FRANK N. VITALJIC
514 13th St., Bellingham, WA 98225.

One common technique applied when converting analog filter functions to digital is the bilinear z-transform, which is given by:

$$s = (2/T_s)(z - 1)/(z + 1).$$

Presented here, however, is a method that eliminates the messy algebra to achieve an equivalent digital filter with the same functional accuracy as the bilinear z-transform.

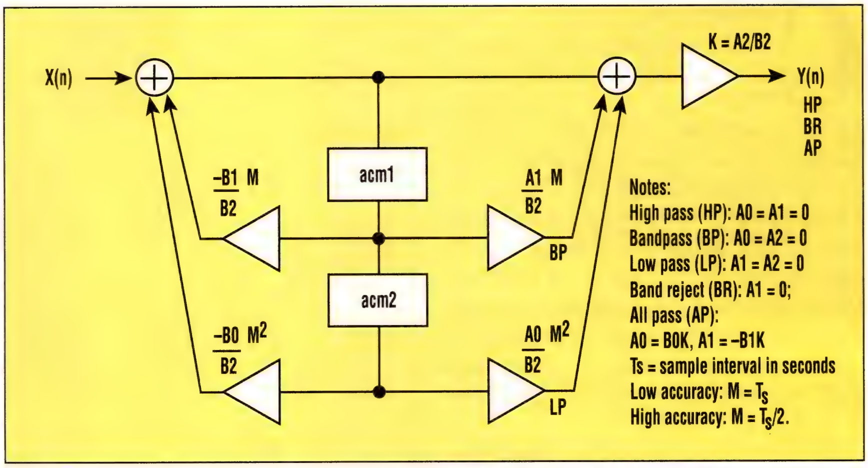
The general analog function H(s) is:

$$H(s) = \frac{(A0 + A1s + A2s^2)}{(B0 + B1s + B2s^2)}$$

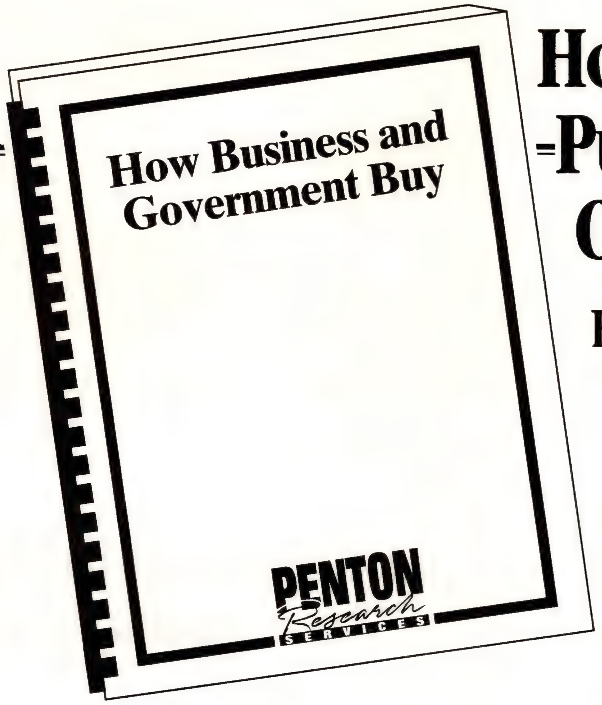
Dividing both the numerator and denominator of H(s) by s^2 results in:

$$H(s) = \frac{K[(A0/A2)s^{-2} + (A1/A2)s^{-1} + 1]}{[(B0/B2)s^{-2} + (B1/B2)s^{-1} + 1]}$$

where K = A2/B2.



1. A GENERAL 2ND-ORDER DIGITAL FILTER uses two accumulators (acm1 and acm2) to implement the five filter types shown plus any user-defined filter. Higher-order filters are realized by cascading these sections.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MSWT-4-20 (Transfer)	DC-2.0	1.8 TX ② 2.0 RX ③	+28 TX ② +27 RX ③	30	3.95

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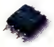

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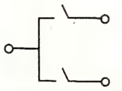

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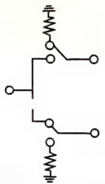

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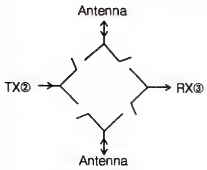

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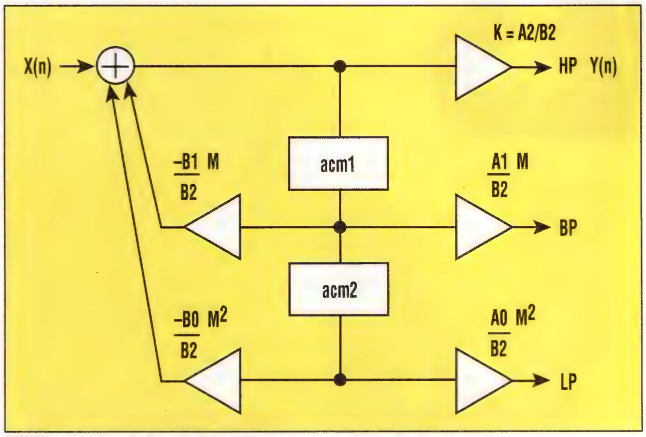

2. A SIMPLIFIED 2nd-order digital filter implements the high-pass, bandpass, and low-pass filter types.

In an analog sense, the second expression is implemented by a filter structure *(Fig. 1)*, with acm1 and acm2 as integrators (1/s). This represents one form of a state variable filter. Integrators can be digitally implemented in one of two ways: rectangular or trapezoidal integration:

Rectangular integration: $\text{out}(n) = \text{out}(n-1) + T_s\,\text{inp}(n)$

Trapezoidal integration: $\text{out}(n) = \text{out}(n-1) + (T_s/2)(\text{inp}(n-1) + \text{inp}(n))$

where T_s is the integration variable.

The output data accuracy is highest with trapezoidal integration. With a sampling-to-data frequency ratio of 8, trapezoidal integration is about 1%; rectangular integration is about 5% *(see the table)*. It can easily be shown that the bilinear transform for integration is identical to trapezoidal integration.

A 2nd-order digital filter is realized with acm1 and acm2 in Figure 1 acting as digital accumulators and the T_s reflected in the filter's coefficients. The points of the structure for the commonly recognized filter types are shown, together with the coefficient constraints. Either low- or high-accuracy filters can be implemented by setting $M = T_s$ or $M = T_s/2$, respectively, along with the appropriate digital-integration algorithm.

For high-pass, bandpass, and low-pass filter types, the filter structure is simplified *(Fig. 2)*. By cascading these filter sections, higher-order filters can be realized. Depending upon sampling rate, filters of order larger than eight should use trapezoidal integration. The Low-Pass Digital Filter Program outlines the statements for a 2nd-order low-pass filter *(see the listing)*. Note that all statements aren't necessary, depending upon the degree of accuracy implemented.☐

SINEWAVE INTEGRATION ACCURACY

	Trapezoidal		Rectangular	
Fs/F	Mean square error	%Error	Mean square error	%Error
4	0.001750	4.18	0.009562	9.78
6	0.000329	1.81	0.003802	6.17
8	0.000103	1.01	0.002056	4.53
12	0.000020	0.45	0.000888	2.98
14	0.000011	0.33	0.000649	2.55
18	0.000004	0.20	0.000390	1.97
24	0.000001	0.10	0.000218	1.48
35	0.0000003	0.05	0.000102	1.01

LOW-PASS DIGITAL FILTER PROGRAM

```
/* set filter coefficients */
  M = Ts;           /* low accuracy only */
  M = Ts/2.0;       /* high accuracy only */

  C2 = (A0/B2)*M*M;
  D1 = (-B1/B2)*M;
  D2 = (-B0/B2)*M*M;

/* reset accumulators */
  acm1 = acm2 = 0.0;
  acm1_old = sumFB_old = 0.0; /* high accuracy only */

/* low pass filter computing loop */
  for(n = 0; n < MAXPTS; n++) {

  /* sum n-th input with feedback samples */
    sumFB = X(n) + (D1*acm1 + D@*acm2);

  /* set filter n-th output sample */
    Y(n) = C2 * acm2;

  /* update accumulators */
    acm1 = acm1 + sumFB; /* low           */
    acm2 = acm2 + acm1: /* accuracy only.  */

    acm1 = acm1 + sumFB + sumFB_old; /* high           */
    acm2 = acm2 + acm1 + acm1_old; /* accuracy only. */
  /* save current states, high accuracy only */
  acm1_old = acm1;
  sumFB_old = sumFB;
  }  /* for */
```

CIRCLE 522

CONTROL AN FSM ENGINE IN SOFTWARE

RON BRAITHWAITE
Software Engineering, 3615 SE Clinton St., Portland, OR 97202;
(503) 231-8620, fax (503) 231-8708.

Many control applications can be defined in terms of a finite state machine (FSM), which has a finite number of inputs that occur in a defined sequence. The FSM can be thought of as an object that performs actions based on a sequence of messages it receives, where the sequence is as important as the individual message.

The FSM structure is made up of a single-byte RAM variable, a ROMed data structure, a very short subroutine for the FSM engine, and the appropriate subroutines to be executed given the defined input.

The ROMed data structure is made up of three tables—state, term, and vector:

- The state table consists of a sequence of bytes that are the offsets from the start of the term table to the first term for the state indicated by the offset from the start of the state table.
- The term table is formed by a series of term entries, which consist of

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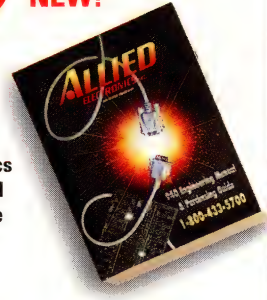

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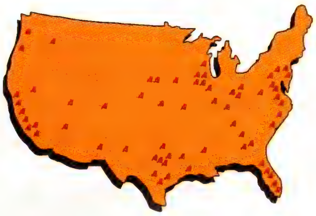

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four values: an input mask, an input match, the next state, and, finally, the offset from the start of the vector table for the subroutine that is to be executed.

- The vector table consists of a series of entries made up of subroutine addresses.

In many cases, the action for most input matches is the same (e.g., no operation). Therefore, if the last field in the term entry is an offset within the term table, it saves a great amount of space.

In cases where there is not much commonality of actions, having the last field be the subroutine address can make the structure smaller as well as slightly faster.

The FSM executes as such: On entry, the FSM uses the value in the current state variable to find the offset in the term table to the first term for that state. Then, the FSM loops through the term entries, masking the input with the input mask and comparing the result to the input match.

If a match occurs, the current state is changed to the next state and the vector table offset is used to indirectly call the entry in the vector table. If the FSM loops through all term entries for the state without finding a match, an exception condition exists.

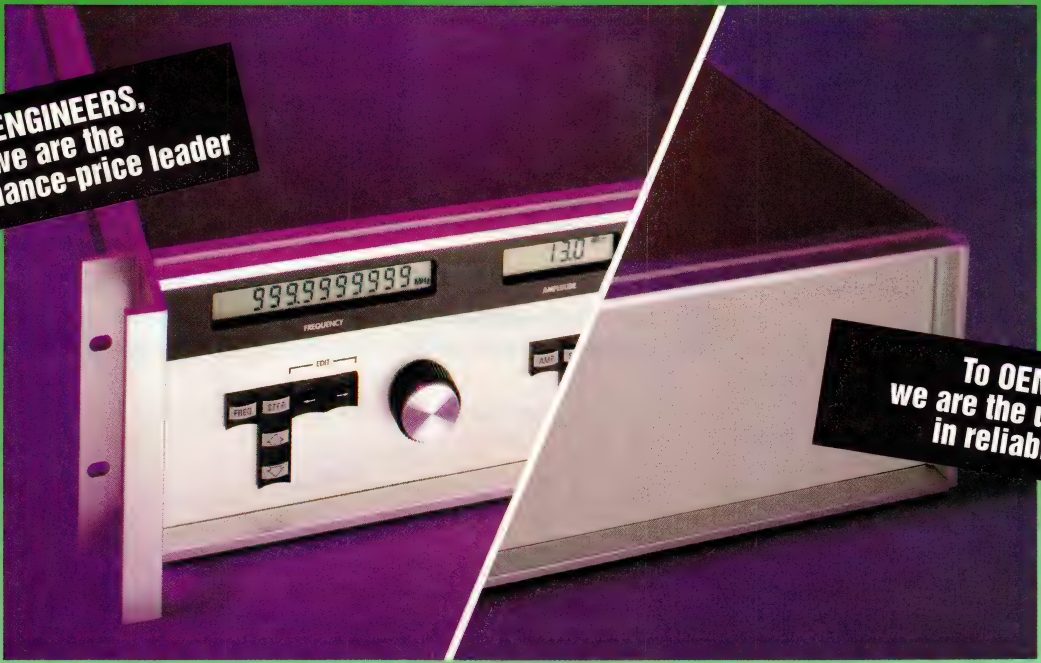
Typically, the last term entry has an input mask of 0 and an input match of 0, allowing an exception handler for that state. An alternative technique can have the FSM execute a general exception handler when there's no match of any term. In this case, the state table entries must be expanded to include a term count for each state.

In the example code listing given, the FSM engine assumes the existence of three tables—states, terms, and vectors—with routines defined to toggle bits in Port A. The cycle count for each instruction is listed in the comment field.

As can be seen from this code, FSMs provide a very fast and efficient technique for handling certain classes of problems. In fact, this mechanism is fast enough to be used at the heart of interrupt service routines, as long as the called subroutines are equally efficient.☐

```
* FSM
*           Call:   A=input                     Return: A=input
*
* Executes a subroutine corresponding to the current state and input.
**********************************************************************************************

            .data

bState:     rmb         1                           ; Current state
            .code

FSM:        psha                                    ; 3 save context
            pshb                                    ; 3
            pshx                                    ; 4

            ldab        bState                      ; 3 get current state
            ldx         #States                     ; 3 get state section
            abx                                     ; 3
            ldab        0,x                         ; 4 get offset to first term
            ldx         #Terms                      ; 3
            abx                                     ; 3
            ldab        #4                          ; 2 size of term entry

fsm1:       psha                                    ; 3 save input
            anda        0,x                         ; 4 input mask
            cmpa        1,x                         ; 4 compare to input match
            pula                                    ; 4 restore input
            beq         fsm2                        ; 3 if equal

            abx                                     ; 3 point at next term
            bra         fsm1                        ; 3 loop

fsm2:       ldab        2,x                         ; 4 set next state
            stab        bState                      ; 4
            ldab        3,x                         ; 4 get offset
            ldx         #Vector                     ; 3
            abx                                     ; 3
            jsr         0,x                         ; 6 go do it

            pulx                                    ; 4 restore context
            pulb                                    ; 3
            pula                                    ; 3
            rts                                     ; 5

States:     db          s0-Terms                    ; offsets to term entries
            db          s1-Terms                    ;
            db          s2-Terms                    ;

Terms:                                              ; term entry table
s0:         db          -1, 0, 0, v1-Vector         ; mask match next offset
            db          -1, 1, 1, v2-Vector         ;
            db          -1, 2, 2, v3-Vector         ;
            db          0, 0, 0, v0-Vector          ;

s1:         db          -1, 0, 0, v1-Vector         ; mask match next offset
            db          -1, 1, 1, v2-Vector         ;
            db          -1, 2, 2, v3-Vector         ;
            db          0, 0, 1, v0-Vector          ;

s2:         db          -1, 0, 0, v1-Vector         ; mask match next offset
            db          -1, 1, 1, v2-Vector         ;
            db          -1, 2, 2, v3-Vector         ;
            db          0, 0, 2, v0-Vector          ;

Vector:                                             ; vector table
v0:         dw          Noop                        ;
v1:         dw          BitA0                       ;
v2:         dw          BitA1                       ;
v3:         dw          BitA2                       ;

Noop:       rts                                     ; do nothing

BitA0:      ldaa        #1                          ; toggle PA0
            staa        PORTA+REGBASE               ;
            clr         PORTA+REGBASE               ;
            rts                                     ;

BitA1:      ldaa        #2                          ; toggle PA1
            staa        PORTA+REGBASE               ;
            clr         PORTA+REGBASE               ;
            rts                                     ;

BitA2:      ldaa        #4                          ; toggle PA2
            staa        PORTA+REGBASE               ;
            clr         PORTA+REGBASE               ;
            rts                                     ;
.END
```

Split Personality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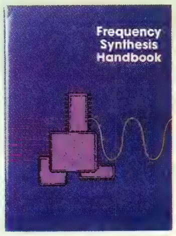

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CIRCLE 523

DETECT RING SIGNALS WITHOUT SPECIAL ICS

PAUL R. WOODS
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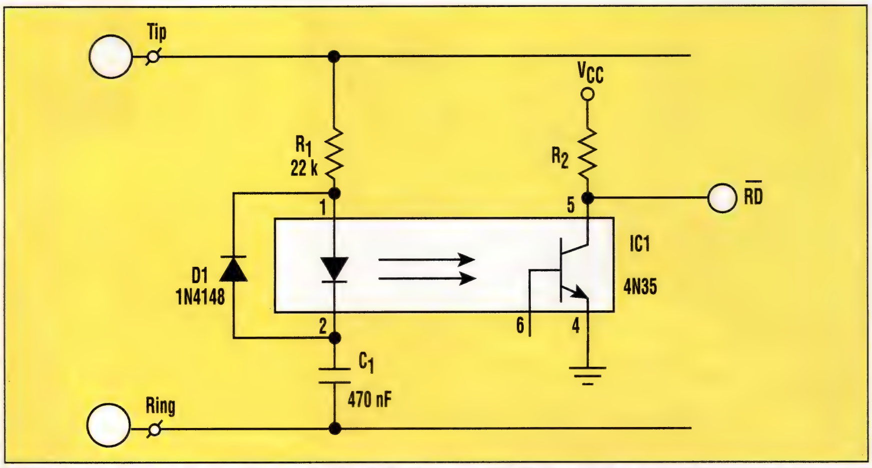
Discriminating between telephone-ring signals and spurious signals on a phone line can be accomplished by using dedicated ICs such as AT&T's LB1006AB or Texas Instruments' TMS1520A. However, if the system already is using a microcontroller, those dedicated chips can be replaced with simpler hardware and a few bytes of code.

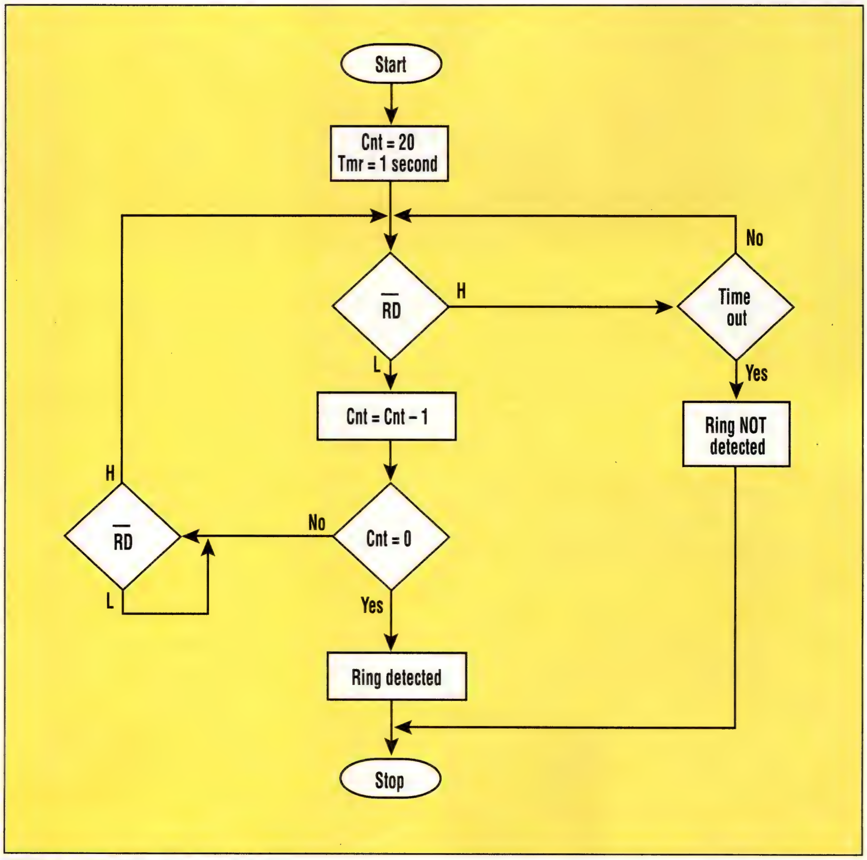
Looking at the setup *(Fig. 1)*, the ringing voltage pulses the optoisolator's LED, which in turn pulses the low-asserted $\overline{RD}$ line to the microcontroller. The firmware analyzes the pulses to determine whether a valid ringing signal is present.

The frequency limits of a valid signal are 20 to 80 Hz, which is modulated 2 seconds on and 4 seconds off (with distinctive ringing, though, this cadence can vary). Therefore, the simplest analysis is to count down at least 20 pulses of $\overline{RD}$ in 1 second *(Fig. 2)*.

The routine could be expanded to determine what type of ring signal is present in a distinctive ring setting. Such a system could switch the phone line to various output jacks. As a result, several phone devices could use the same line without first picking up the line to determine if it's a voice, fax, or data call.☐



1. DETERMINING TELEPHONE RING SIGNALS and spurious signals on a phone line is possible without dedicated chips if the system already employs a microcontroller. The chips can be replaced with simpler hardware and a few lines of code.



2. THE DIAGRAM illustrates the simplest way to analyze the 20-to-80-Hz frequency limits of a valid signal that's modulated 2 seconds on and 4 seconds off: Count down at least 20 pulses of $\overline{RD}$ in 1 second.

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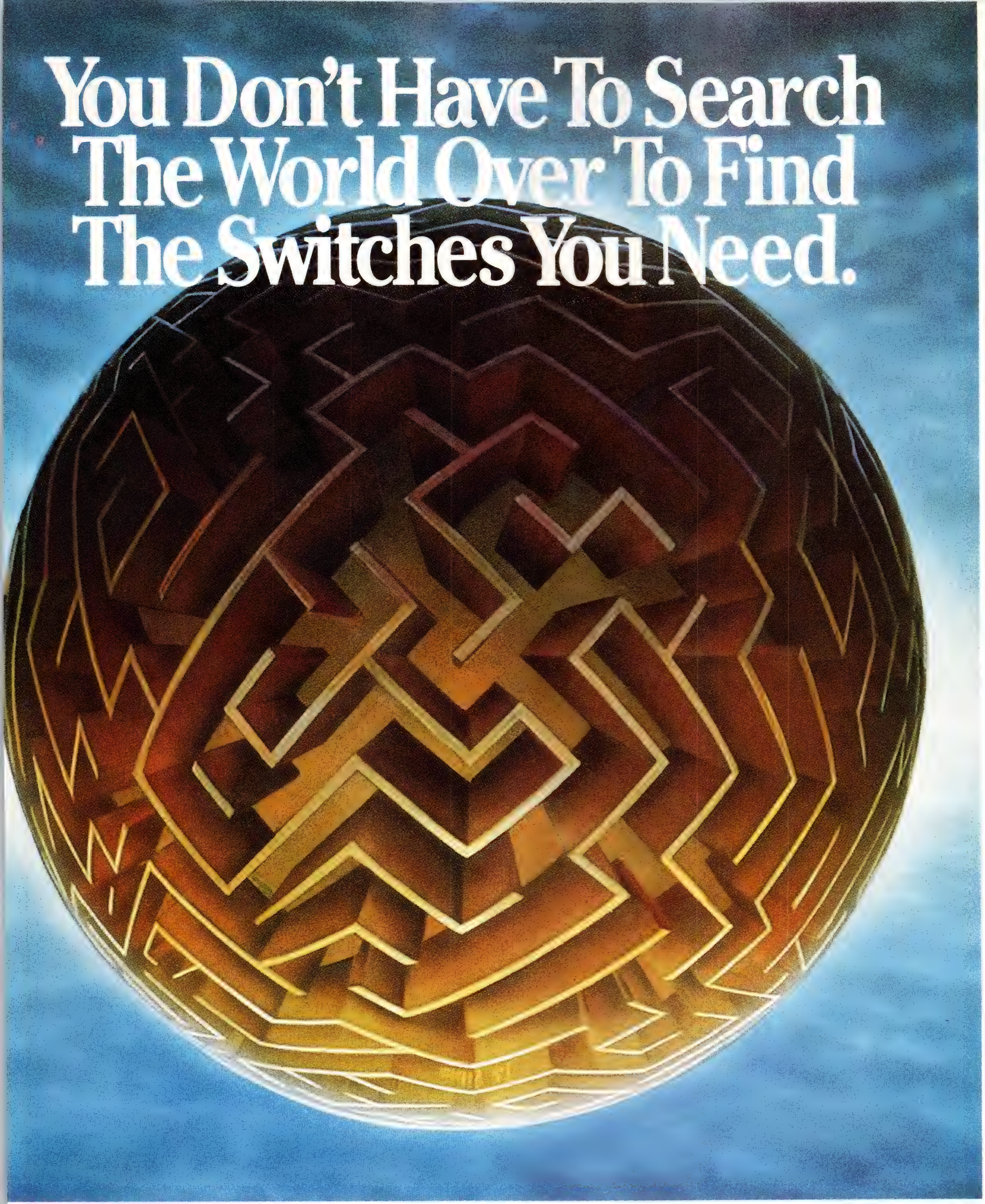
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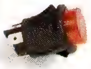
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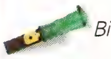
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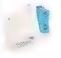
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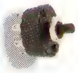
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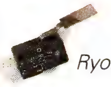
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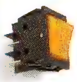
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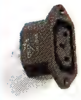
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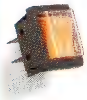
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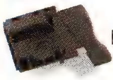
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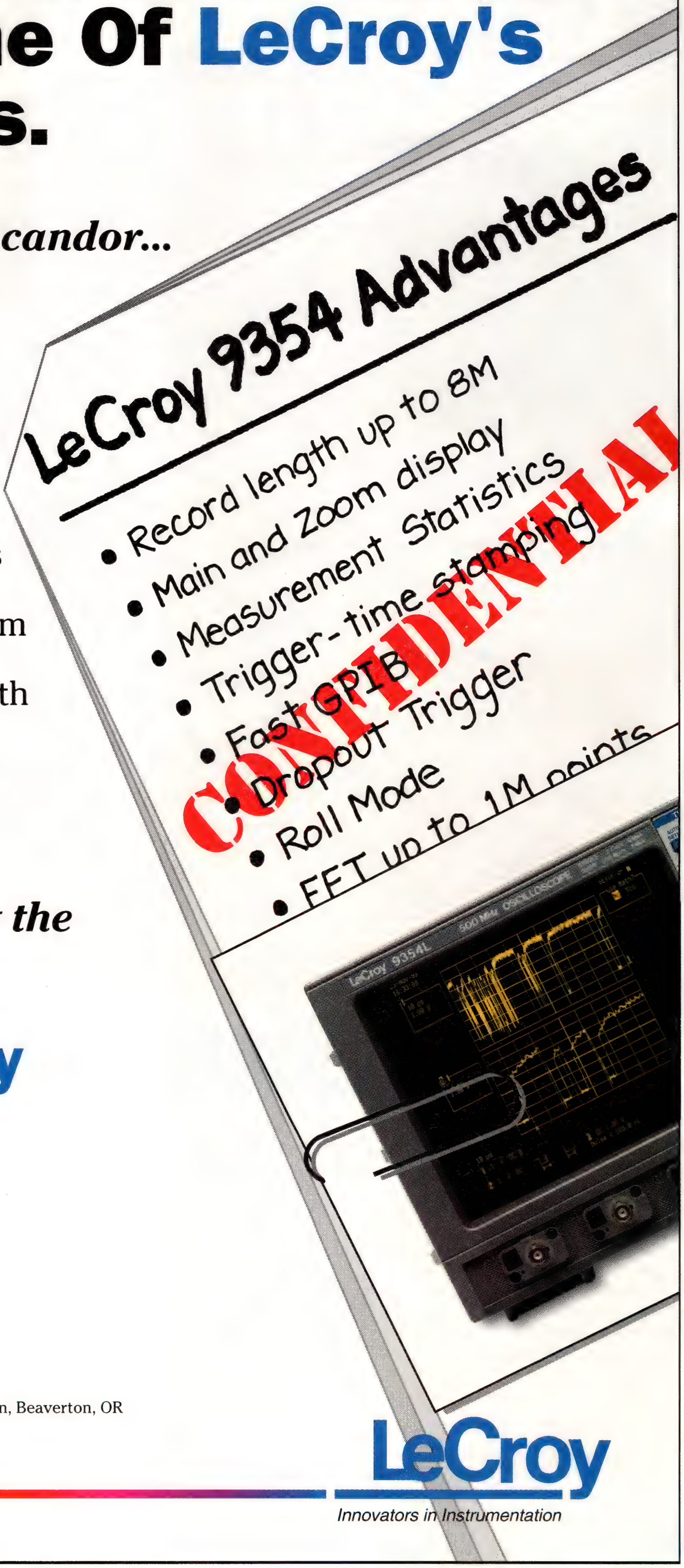

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PEASE PORRIDGE

BOB'S MAILBOX

Dear Mr. Pease:

We are a garage operation startup that has just received a federal SBIR (Small Business Innovation Research) phase I grant to develop and evaluate several nontraditional tactile imaging sensors. Our literature search turned up two old magazine articles authored by Dudley B. Clark, Clark Electronic Labs, Palo Alto, Calif. In them, Mr. Clark talks about his proprietary piezoresistive pressure sensors that have a world of desirable features, e.g. large dynamic range, good resistance to overpressure damage, little hysteresis, low (and linear) thermal drift, little aging drift, good sensitivity and repeatability, lots of output ranging options, etc.

The implication is that the materials employed change their fundamental resistivity when loaded (stressed). If true, this is quite different from those sensing technologies which depend on changes in internal connections, path length, and/or cross-section. Such sensors seem almost too good to be true.

Clark said that his sensors were made of intermetallic "plastic" materials composed of zirconium tetrachloride and rare earths (presumably scandium, yttrium, and the lanthanide series elements or their compounds). I would like to include evaluation of Clark's technology as part of our SBIR if more information can be obtained from Mr. Clark, his associates, his firm, its successor, or any other source. Unfortunately, time is short.

So far, I cannot find hide nor hair of D.B. Clark or his firm. As you might expect, the publishers of the magazines have no records dating back to the '50s and '60s.

If you or any of your readers can shed any light on this subject, I can be reached at (612) 881-2824.

D. CAMERON SMITH
The Oxboro Technical Group Inc.
Bloomington, Minn.

Does anybody know the whereabouts of Mr. Clark? Or where his technology may reside?—RAP

Dear Bob:

I was pleased to see your column in the May 2 issue about the oversimplification that is so often seen in the JIT process. Let me tell you my experience.

I started with a major instrument manufacturer in Beaverton, Ore., in 1977. During that time, it was difficult to get parts. They either couldn't get the inventory they needed, or couldn't efficiently distribute the inventory to where it was needed. So, in the early '80s, they built an "automated warehouse" with a vast capacity for components in computer-picked storage bins. They got the process up and running, and eventually perfected their component delivery system. Then they got the JIT religion. A few years later, they held an auction to try to sell off a large number of assets (reducing staff from about 25K to 8K left them with a lot of extra stuff). As I recall, nobody even put in a bid for the storage system.

It is possible that the high-level people understand the complex factors involved in optimizing inventory. But the low-level people who actually buy the parts do not. A plastics manufacturer was saying that he sells them a small part, a year's supply of which would fit in the palm of your hand and cost 5 cents each. Instead they insist on buying these parts a week's supply at a time at 50 cents each. This JIT is not costing them "a little bit more," but "A LOT MORE," at least on some items. It has been suggested they buy through distributors, who would hold stock for them at little additional cost. But that is contrary to the JIT religion, so they won't do it.

The problem with the JIT method is that it compromises profit margins forever, or at least from the moment JIT is implemented until it is abandoned. Every year, those higher JIT materials costs cut into the gross margin. Tightening inventory through JIT releases cash from the balance sheet only once, as a one-time event occurring at implementation of the JIT program. From then on, JIT impairs profitability every month of every year. Only a very shortsighted management team could expect to prefer a one-time cash-flow boost over long-term income statement profits.

Since then, I've started a small company, and our inventory decisions are not based on religious zeal. We consider our usage rate, how long it will take to get additional stock, physical size of the part, quantity pricing discounts, availability from alternate sources, item cost and margin, and whether this is a critical part of a larger system versus a minor accessory.

If sales shoot up, we can build up and ship from stock until replacement materials arrive. If sales are slow, well, we have some money tied up in inventory. But I would rather we make continuing profits from sales of product (which leads to repeat sales, larger market share, and a more stable income stream), than from manipulating inventory to extract cash once (which leads to inability to meet demand, and loss of sales).

When we introduced our first product nationally, we were overwhelmed with demand. On many parts, we found that we had bought up all of the available inventory in the whole country! It is disheartening to call the largest North American distributors and find that their total nationwide stock of a critical part is fifty pieces. Since then, we have set up a relationship with a couple of smaller distributors to carry extra stock of critical components, so that even during a surge in demand we will not run out of stock. They get most of our semiconductor business.

Bob, I think that part of our frustration is that as engineers, we see the world as a bunch of tinker-toys that can be put together in various ways to achieve the results we want. Buyers can be clerical types who are used to strictly adhering to policies and rules, leaving little room for personal decision making. And senior managers are sometimes so driven to achieve quar-

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PEASE PORRIDGE

terly goals that they make decisions which sacrifice long-term success.

RONALD M. JACKSON
Chief Engineer
Fascinating Electronics Inc.
Beaverton, Ore.

I agree, statements that JIT saves money are SUSPECT. Seems to be a case of "proof by repeated assertion." If the world were a LINEAR place, the apples-and-oranges types would be heroes. But the world is NOT a linear place. Life ain't fair. (!&*@% the bean counters.)—RAP*

Dear Mr. Pease:

Your column in the May 30 issue, "*What's All This Teledeltos Stuff, Anyhow?*," was interesting. You mentioned having difficulty finding conductive paint.

A recent problem with my telephone led me to find a conductive paint pen that works very well. The flexible circuit board that is used behind the keypad developed some open circuits. The plastic obviously doesn't take to soldering without melting, so the only way to repair the traces is with a conductive paint. A few weeks before this incident, I had noticed a conductive paint pen available at Halted Specialties, 3500 Ryder St., Santa Clara, Calif. This pen makes it very easy to apply the paint just where you need it.

The pen is called the "Circuit Works" conductive pen model 2200 and costs about $11.00. The company that manufactures the pen is Planned Products, located at 303 Potrero St., Suite 53, Santa Cruz, Calif.

PAUL N. LEONARD
Sr. Controls Engineer
Matheson Electronic Products Group
San Jose, Calif.

Exactly! That's another good way to repair conductors that don't like to be soldered—and to contact onto Teledeltos paper.—RAP

All for now. / Comments invited!
RAP / Robert A. Pease / Engineer

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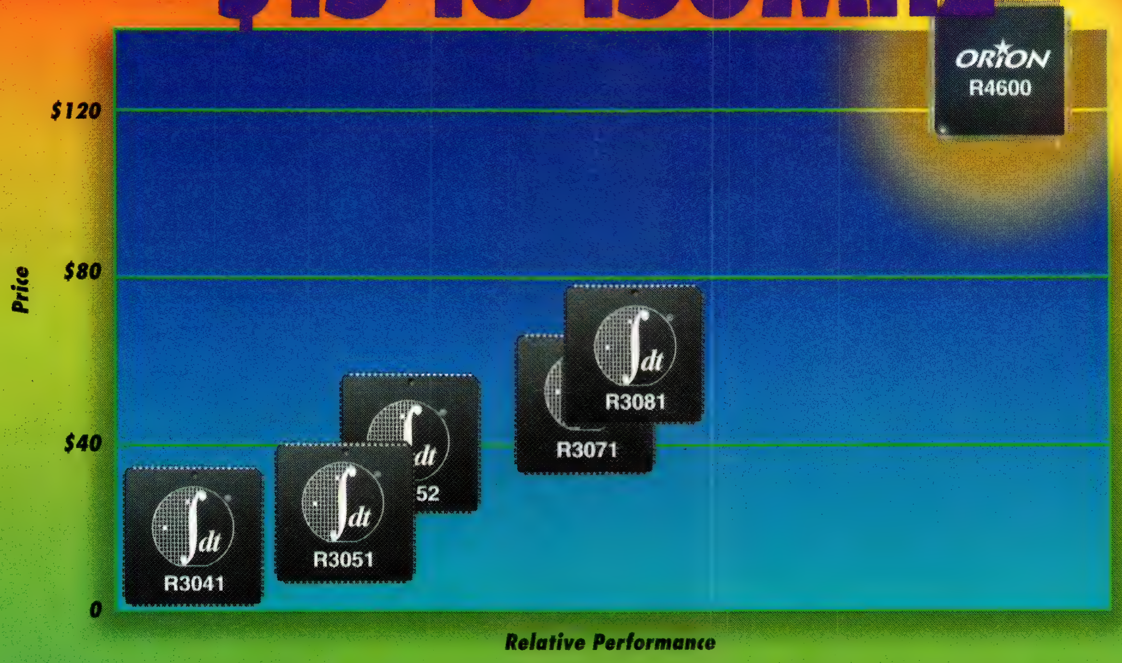

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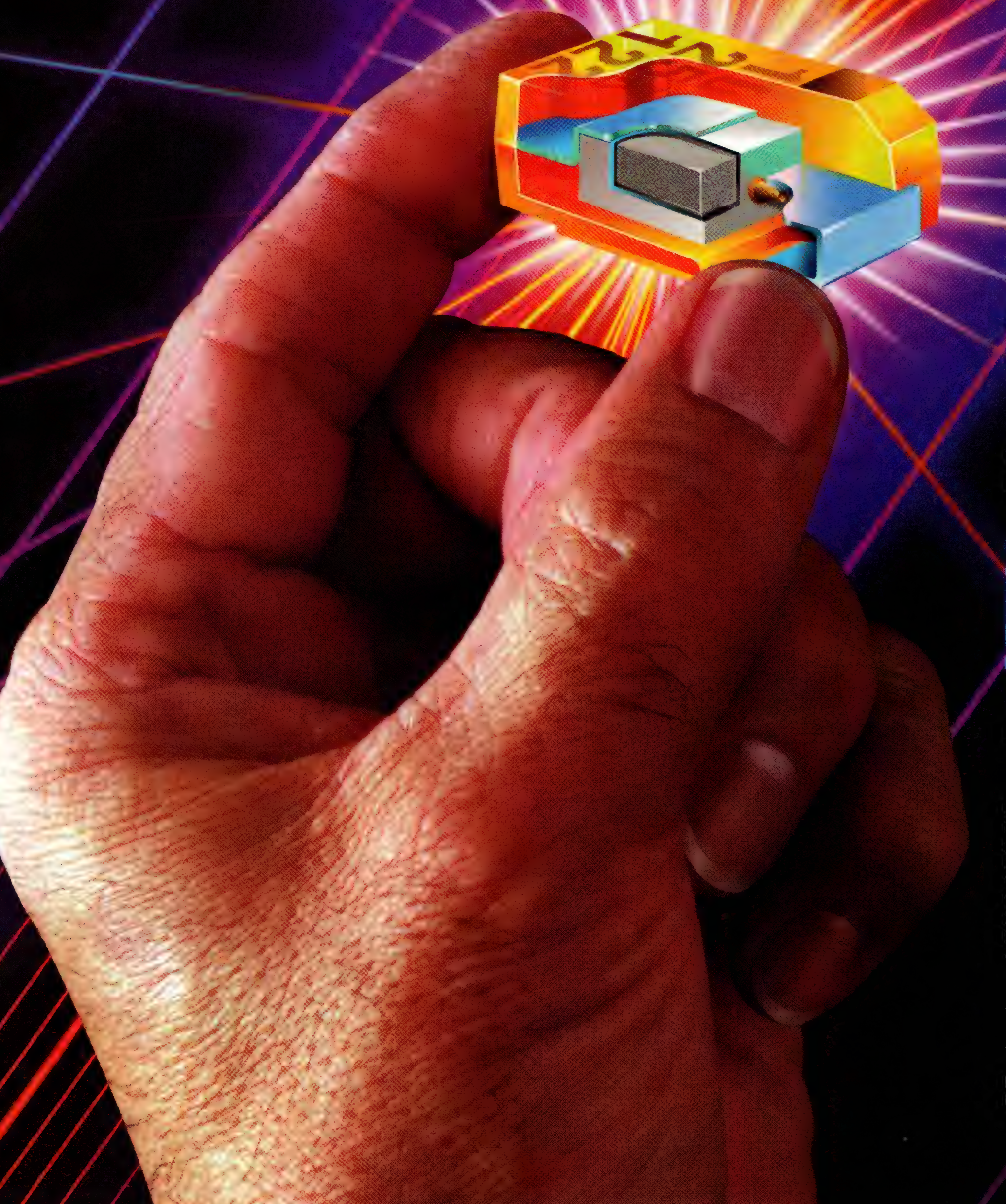

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A SPECIAL EDITORIAL FEATURE

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ELECTRONIC DESIGN

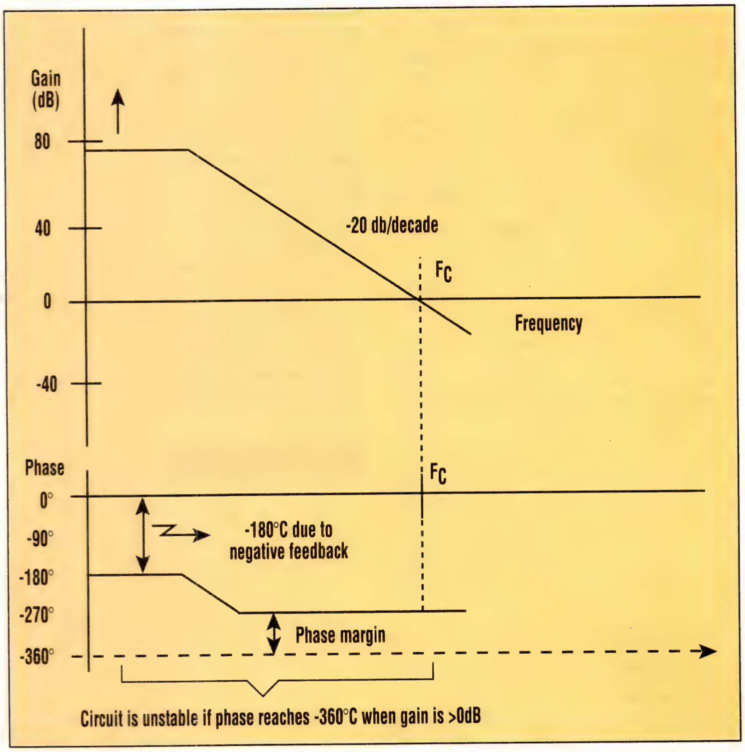
Understanding Linear-Regulator Compensation

Here's how to specify the right value for a linear regulator's output capacitor.

BY KIERAN O'MALLEY

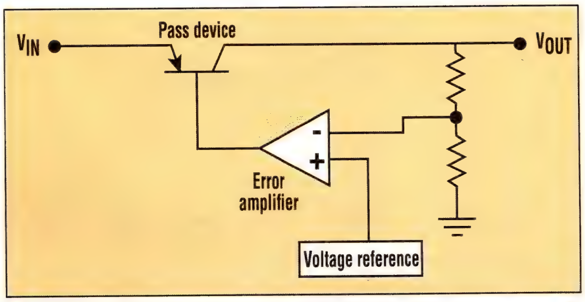
Cherry Semiconductor Corp., 2000 S. County Trail, East Greenwich, RI 02818; (401) 885-3600.

In most cases, the data sheets that describe linear regulators do not adequately cover the role of the output or compensation capacitor. Although compensation is typically associated with switching regulators, it's also a requirement with low-drop and composite linear regulators. A standard or npn regulator generally doesn't need an external compensation capacitor because of the superior frequency response of the npn pass device. But in most low-drop or composite regulators, the pass device or pass-device driver is a lateral pnp transistor. Such transistors are inherently low-frequency cutoff devices, resulting in a poor transient response for the regulator. Hence the need for an external capacitor connected between the output and ground to provide filtering and compensation.



Circuit is unstable if phase reaches -360°C when gain is >0dB

2. Any feedback system should have a closed-loop response that ensures unconditional stability. The ideal system has a single-pole response at crossover.



1. A low-drop linear regulator comprises a voltage reference, an error amplifier, and a series pass device.

For most designers, information on the choice of an output capacitor comes from the applications section of the regulator data sheet, which typically contains a statement such as "an output capacitor is required for stability." This is accompanied by a suggested value, with 10 μF being the favorite. Often, the designer uses the capacitor value given in the application diagram without worrying about how it was arrived at. This capacitor is not necessarily the most cost-effective or best solution for a particular application.

The output or compensation capacitor determines three main characteristics of a linear regulator: start-up delay, load transient response, and loop stability. Too large a value of capacitor requires a longer time to charge fully. On the other hand, a completely discharged output capacitor will cause the regulator to current limit at start-up. The start-up delay is:

$T_{start} = CV_{out}/I_{limit}$

Too small an output capacitor can result in overshoot on start-up, because the capacitor can charge to a high voltage before the control loop can respond. This is a problem if the regulator is powering sensitive logic or microprocessor circuitry where excess voltage can cause damage. Because it's impossible to examine all three characteristics at once, the designer should concentrate on achieving a stable loop design. The start-up delay and load transient response can be checked later.

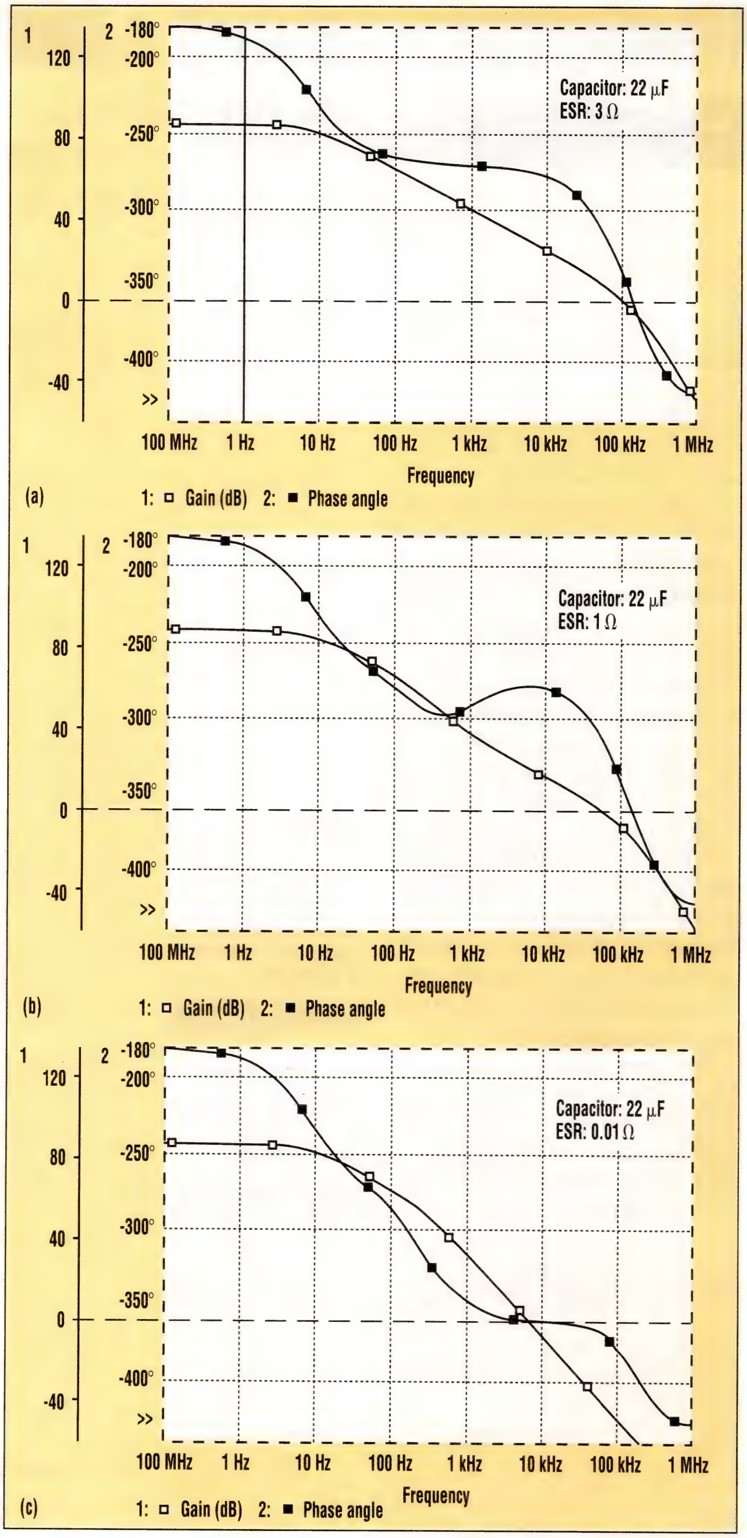
For compensation, use a capacitor with a low impedance over a wide frequency range. For load transient response, select a low ESR. The value should also make for a reasonable start-up delay.

As a simplified block diagram of a low-drop linear regulator shows, the device consists of three basic parts *(Fig. 1)*. For one, there must be a voltage reference that's independent of temperature and supply voltage. There must also be an error amplifier to compare the voltage reference to a sample of the output voltage and to generate a signal proportional to their difference. The third major component is a series pass device to provide current to the load and regulate the output voltage.

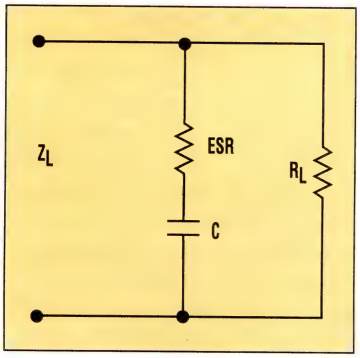
Any feedback system should have a closed-loop response that ensures unconditional stability. The ideal system has a single-pole response at crossover *(Fig. 2)*. The crossover frequency should permit quick response to load transients. The phase margin should be above –180° at all the lower frequencies.

In reality, however, a low-drop linear regulator typically has three dominant poles, two of which are fixed by the design of the regulator IC. The first of these is determined by the error amplifier and generally occurs at frequencies between 10 and 300 Hz. The second internal pole is due to the pnp pass device or to the pnp bias device in a compound regulator. It occurs at a frequency between 100 and 300 kHz, depending on load.

The third pole results entirely from the load on the regulator and the output capacitor. The higher the load current, the higher this pole will be in frequency for a given regulator. Therefore, at light loads, this pole may be lowest in frequency. A simplified load for a regulator is shown *(Fig. 3)*. The transfer function is:



4. Three Bode plots show the effect of the output capacitor's ESR on gain and phase margin. The test regulator is Cherry's CS-8156 dual device and the capacitor value is 22 μF. With an ESR of 3 Ω on the 12-V output, there's only 10° of phase margin (a). Reducing the ESR to 1 Ω increases the phase margin to about 35° and gives a gain margin of about 20 dB (b). A "perfect" capacitor with ESR of 0.01 Ω, however, may cause a problem with loop stability. Gain falls to zero at about 8 kHz with almost no phase margin (c). Hence, it's best to use a tantalum or aluminum electrolytic capacitor for compensation rather than a film capacitor, which may have too low a value of ESR.



3. Of the three dominant poles for a low-drop linear regulator, two are fixed by the design of the regulator IC. The third pole results entirely from the load on the regulator and the output capacitor, which is shown here in a simplified schematic.

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$$Z_L(s) = \frac{\left(ESR + \frac{1}{sC}\right) \times R_L}{R_L + ESR + \frac{1}{sC}} \qquad (1)$$

$$Z_L(s) = \frac{R_L(1 + ESR \times sC)}{1 + sC(R_L + ESR)} = \frac{(1 + Z_1)}{(1 + P_1)} \qquad (2)$$

The pole added by the load is at a frequency given by:

$$f = \frac{1}{2\pi(R_L + ESR)C} \qquad (3)$$

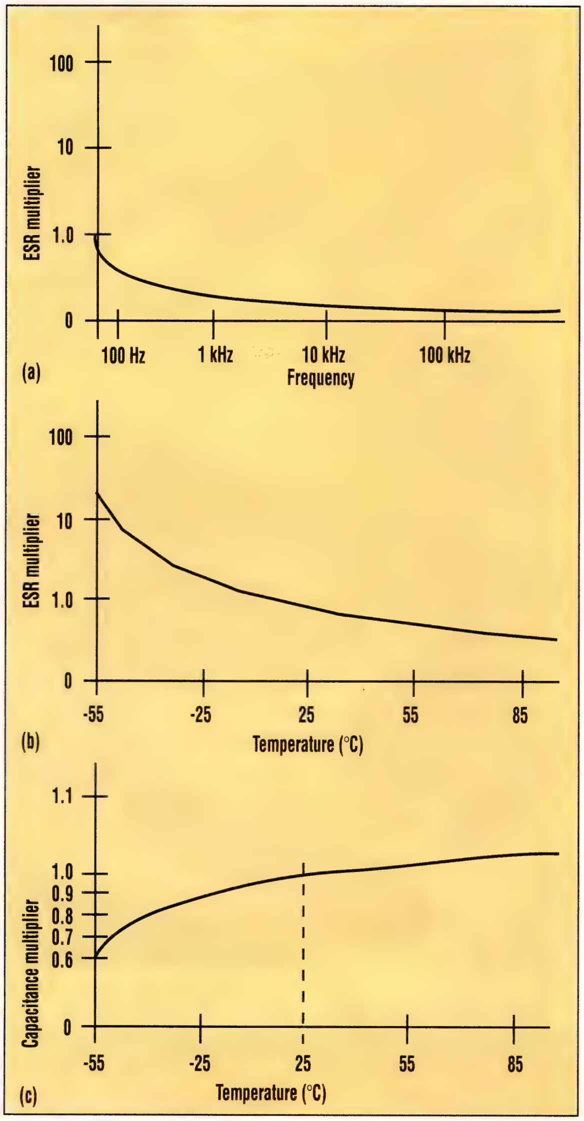
where R_L is the load, which, for example, may be 12 V at 250 mA. In that case, $R_L = 48\ \Omega$. Obviously, this pole moves depending on the load, and its range of movement depends on the output capacitor.

The ESR of the output capacitor adds a zero to the loop at a frequency given by:

$$f = \frac{1}{2\pi(ESR)C} \qquad (4)$$

A capacitor with a high ESR value creates a zero at a low frequency close to the error amplifier or the load pole and cancels the effect of one of them. This gives a one-pole response but with significant gain up to higher frequencies. Using such a capacitor can result in insufficient phase margin and instability.

5. Three graphs show typical capacitor characteristics. ESR is plotted versus frequency (a) and temperature (b), while capacitance is shown versus temperature for a typical electrolytic device (c). These variations are usually less for capacitors with higher voltage ratings but depend primarily on capacitor type and manufacturer.



A Spice run shows the Bode plot of Cherry's CS-8156 dual regulator. The output capacitor is a 22-μF device with an ESR of 3 Ω on the 12-V output that leaves only 10° of phase margin *(Fig. 4a)*. When the ESR is reduced to 1 Ω, phase margin rises to about 35° and a gain margin of about 20 dB is added *(Fig. 4b)*. Output current and ambient temperature are 100 mA and –40°C in each case.

A perfect capacitor (almost zero ESR) may also cause a problem with loop stability because the zero due to the ESR is at a high frequency. The gain slope falls at a rate of –40 dB per decade (–2 slope) to 0 dB before the capacitor zero can affect the slope. Another Spice plot illustrates this problem using a "perfect" 22-μF capacitor on the output of the CS-8156 dual regulator *(Fig. 4c)*. The gain falls to zero at about 8 kHz with almost no phase margin. For this reason, it's best to use a tantalum or aluminum electrolytic capacitor for compensation rather than a film capacitor, which may have too low a value of ESR.

The system designer will not be able to tell exactly where the internal poles are for a given regulator. He will, however, be able to tell if the loop is stable by observing the regulator's output.

A design's stability depends on the following factors:

1. *Output-capacitor value:* A higher value of output capacitor will make the regulator more stable.
2. *Capacitor ESR:* In general, a capacitor with low ESR will improve the design's stability. But too low a value of ESR can theoretically cause instability.
3. *Load current:* Most regulators are more unstable when operated in their low-to-medium load range, such as 100 mA for a 500-mA regulator. Fast changes in load current can also cause instability.
4. *Temperature range:* At lower temperatures, the loop gain increases. In addition, the capacitor ESR rises while the capacitance value falls, making the design more unstable.
5. *Supply voltage:* At higher input voltages, the loop gain tends to increase, adding to instability.

The output current, temperature, and supply-voltage range are all known for a particular application. Therefore, the design's stability ultimately depends on the choice of capacitor.

A capacitor value and type can be chosen based on cost, availability, size, or temperature constraints. A good starting point is the IC manufacturer's recommended value. If possible, start with a tantalum capacitor of the recommended value and work toward a less costly solution. Often overlooked by designers is the fact that a capacitor is affected by temperature, which can cause large variations in capacitance value and ESR.

The ESR changes the impedance of the capacitor. It has the same effect as adding an external resistor in series. In an aluminum capacitor, the ESR varies slightly except at low temperatures, where it can increase by a factor of up to 30 times. Most aluminum capacitors are unsuitable for applications where they are likely to be exposed to temperatures below –40°C. If the design must work at high temperatures, the capacitor must be rated accordingly. Many aluminum electrolytic capacitors only work to 85°C.

Typical capacitor characteristics over temperature and frequency are shown *(Figs. 5 a, b, and c)*. These variations are usually less for capacitors with higher voltage ratings but de-

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pend primarily on capacitor type and manufacturer.

The first step in determining the correct output capacitor is to place the completed circuit (with a tantalum capacitor of the manufacturer's recommended value) in an environmental chamber set to the lowest specified operating temperature and monitor the output on an oscilloscope. If no capacitor is recommended, begin with 10 μF. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum electrolytic capacitor.

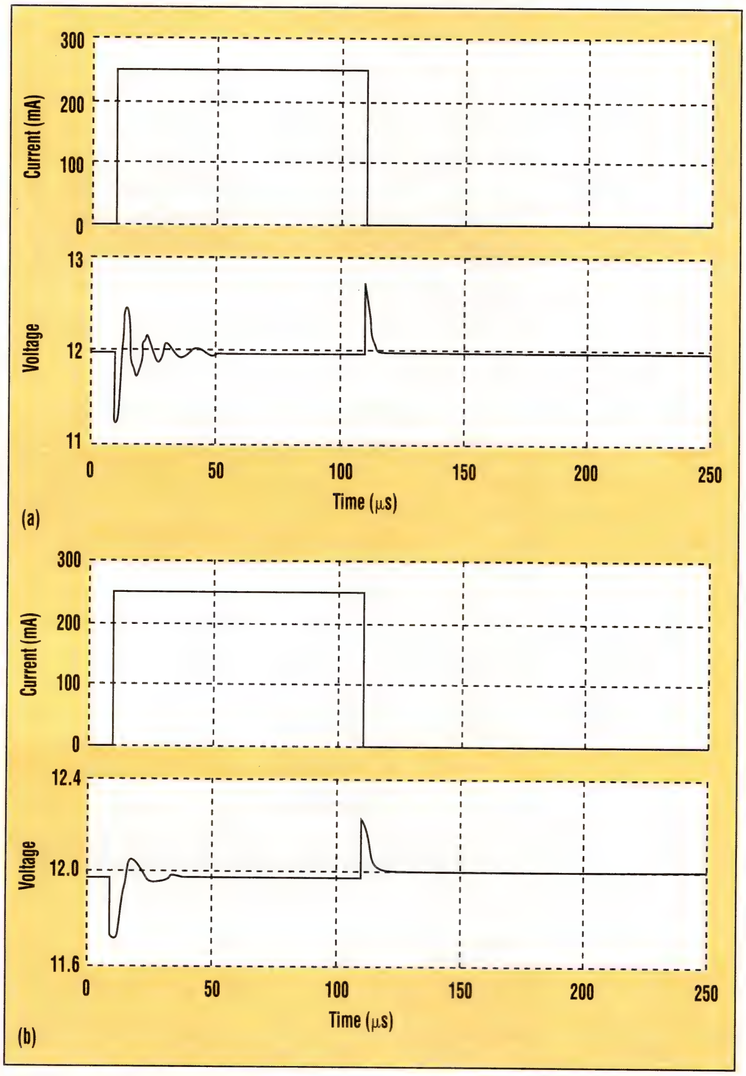
With the input voltage at its maximum, slowly increase the load current from minimum to maximum while watching the output for any oscillations. This confirms that the capacitor is large enough to ensure stability under steady-state conditions.

Next, increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations begin. Record the values of load current and ESR that cause the greatest oscillation. This is the worst-case load condition for the regulator at low temperature. Then vary the input voltage while maintaining worst-case load conditions to see if the oscillations increase. Go up or down to the next standard capacitor value and repeat the manipulations of ESR and load current to optimize performance.

Then, test the load transient response by switching in various loads at several frequencies. This will determine the stability of the design in a real working environment. The load and frequency should be compatible with what the regulator will see in its actual application. Vary the ESR to reduce the ringing. The Spice plots in Figs. 6 a and b show the transient response of the CS-8156 regulator using a 22-μF capacitor with an ESR of 3 Ω and 1 Ω, respectively.

Remove the unit from the environmental chamber and heat the IC using a heat gun to see if the oscillations increase with temperature. Vary the load current to see if the design oscillates. With most regulators, cold temperatures cause trouble, but it's best to find out now.

With the minimum capacitor value and maximum ESR established, a safety factor should be added to allow for the tolerance of the capacitor and for any variation in regulator performance. Most good-quality aluminum electrolytic capacitors have a tolerance of ±20%. Therefore, the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum ESR found.



6. When testing for load transient response, the load and frequency should be compatible with what the regulator will see in its actual application. Vary the ESR to reduce the ringing. Spice plots show the transient response of the CS-8156 regulator using a 22-μF capacitor with an ESR of 3 Ω (a) and 1 Ω (b).

References:
Motorola Inc., Linear/Switchmode Voltage Regulator Handbook, 2/89, Rev. 3
Simpson, Chester, "Understanding Three-Terminal Regulators, *Electronic Design*, Jan. 21, 1993, p. 77.

Special thanks to Bob Lanoue, George Schuellein, and Paul Sisson of CSC.

Kieran O'Malley is an applications engineer at Cherry Semiconductor Corp. Originally from County Mayo, Ireland, O'Malley holds a BSEE from the University of Limerick.

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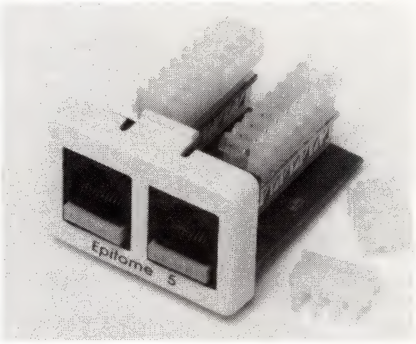

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(continued on p. 130)

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(continued on p. 132)

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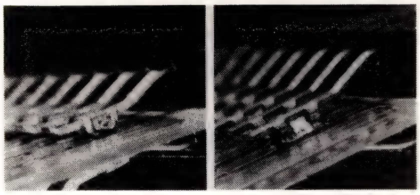

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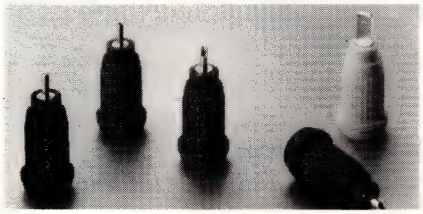

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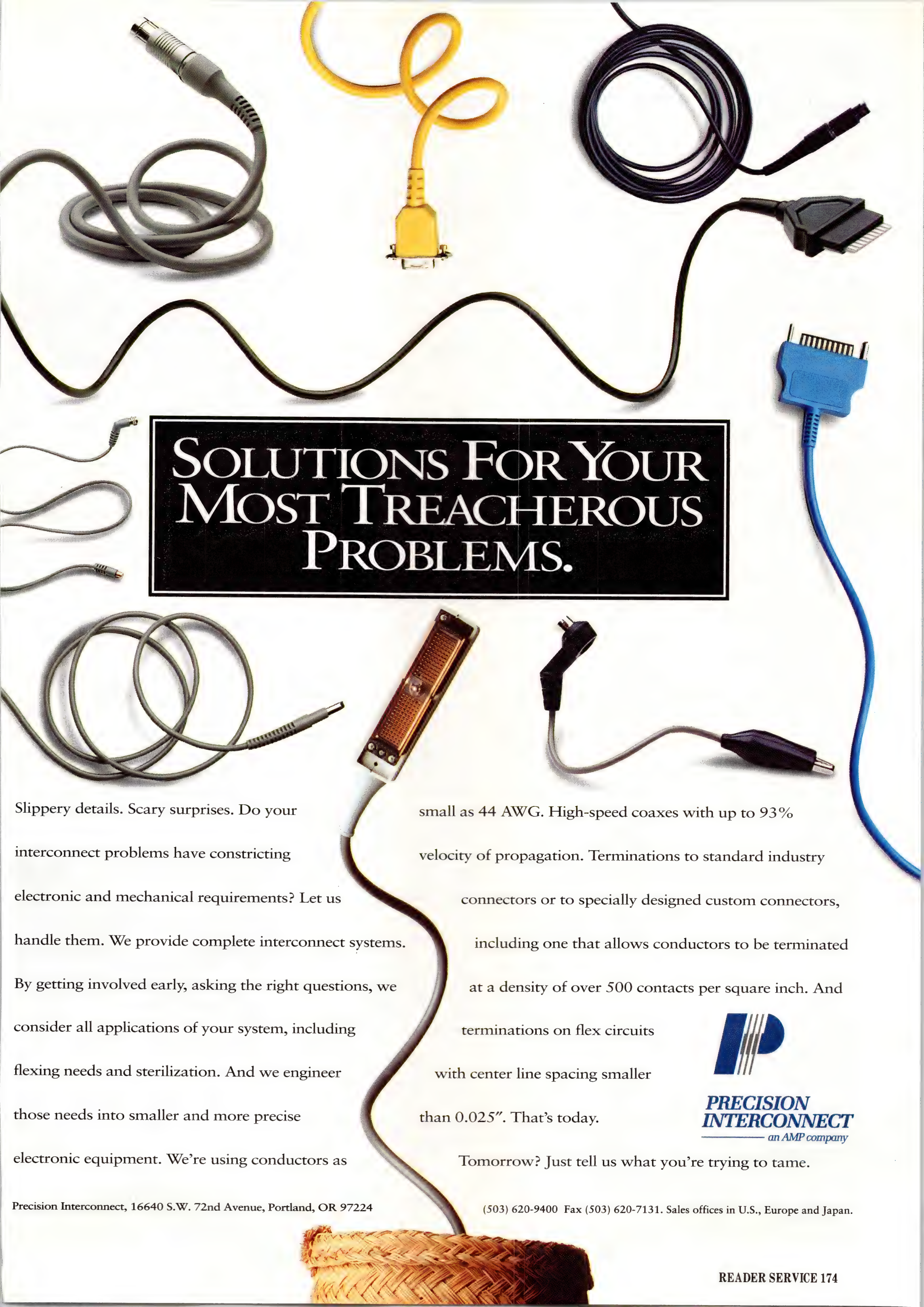

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(BU) (GB) (GP) (VR) (PT)
(EM) (MI) (CM)
CIRCLE 881

Nemal Electronics Inc.
12240 N.E. 14th Ave.
North Miami, FL 33161
(305) 899-0900
(AU) (RF) (CX) (CO) (TW)
(SH) (HK)
CIRCLE 882

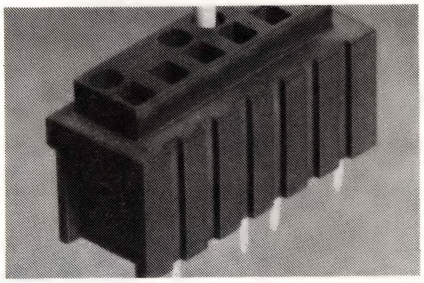
ODU U.S.A.
Sub. of Otto Dunkel GmbH
4620 Calle Quetzal
Camarillo, CA 93012-8558
(805) 484-0540
(AU) (CX) (DS) (DI) (FC)
(CE) (ID) (ZI) (SM) (CD)
(MD) (BI) (HC) (RP)
CIRCLE 883

Optima Electronic Packaging Systems
2166 Mountain Industrial Blvd.
Tucker, GA 30084-5088
(404) 496-4017
(BP) (GP) (CN) (IN) (VR)
(EM) (MI) (CM) (ER)
CIRCLE 884

(see p. 136 for key)
(continued on p. 134)

▼ PC-BOARD CONNECTOR TRAPS STRIPPED WIRING

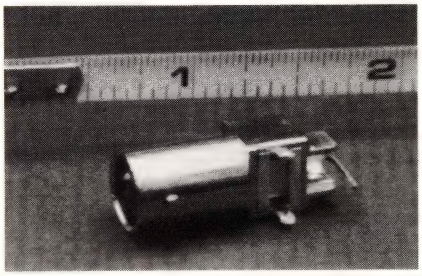
An easy-to-connect pc-board Wire-Trap connector mates with the stripped end of 16 and 18 AWG solid and 18 and 20 AWG stranded wire. The BA-2675-XXX-X right-angle and BA-2634-XXX-X vertical connectors feature a contact design that provides for rapid, simple field installation. Ratings are 6 A per circuit at 600 V ac and units are available in from three to 10 positions. Call for pricing and delivery.



Methode Electronics Inc.
Interconnect Products Div.
1700 Hicks Rd.
Rolling Meadows, IL 60008
(800) 323-6864
▶CIRCLE 615

▼ LOW-PROFILE BNC JACK IS FULLY SHIELDED

Featuring the lowest profile available, a right-angle BNC jack is well suited for use in 10Base2 LAN interconnections, radio telecommunications, broadcast and medical equipment, computers, precision video, and test instruments. The fully shielded jack is constructed of a zinc alloy that's then plated with nickel. Phosphor-bronze contacts are plated with 15 μin. of gold. Pricing is \$3.50 in small quantities. Delivery is from stock.



Bomar Interconnect Products Inc.
1850 Route 46 East
Ledgewood, NJ 07852
(201) 347-4040
▶CIRCLE 616

WE POWER YOUR STRONGEST IDEAS.

When Techron began making power amplifiers in 1951, we had no idea how such technology would come to impact human life. What began as the power source for the music industry grew into the wellspring for some of mankind's greatest achievements and most exciting new developments. A pathway to which Techron is fully dedicated.

Techron's reputation for creating a reliable high-power source led first to industrial and medical applications. A leading blue-chip company required the power, speed and fidelity to power Magnetic Resonance Imaging systems that only a Techron amplifier could provide. Techron responded with a custom product that supplied the gradient sub-system with precise, controlled, reliable power day after day.

The Techron spark of ingenuity has paved numerous inroads to a better way of life. After MRI applications came many exciting new fields of research. Most recently, research to make other medical procedures safer and less painful. The clean, steady reliability of Techron power is there.

Techron's influence has been truly far-reaching. In chemical analysis, expanding the ways X-rays create images. Guiding new ways of thinking in space exploration. Powering oil exploration. Vibration test systems. Quality assurance testing for transformers, capacitors and cable harnesses. Recycling methods. Radar installations. Automotive research for safer vehicles of the future. Safer mining by underground signalling. Particle acceleration studies. Noise-reduction research. Digital simulation to test protective relays used by the electrical power generation and transmission companies.

It started with a product: Strong, clean, reliable power amplifiers. But it grew to fuel a generation of strong new ideas that not only are improving our lives today, but building a better future. We're proud to be a part of it. And we're committed to staying here. Right behind your greatest ideas. For literature call 1-800-933-7956.

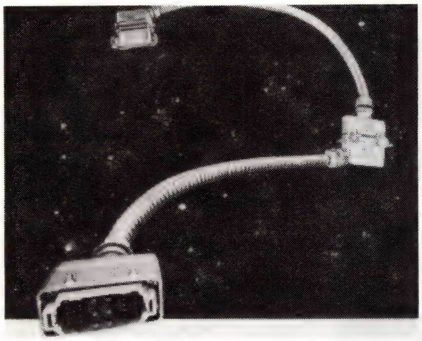
TECHRON®

1718 West Mishawaka Road, Elkhart, Indiana 46515 -1000
(219) 294-8300 for Sales and Applications Engineers
Techron is a division of Crown® International Inc.

READER SERVICE 179

▼ CONNECTOR COMBINES FIBER, WIRE IN ONE

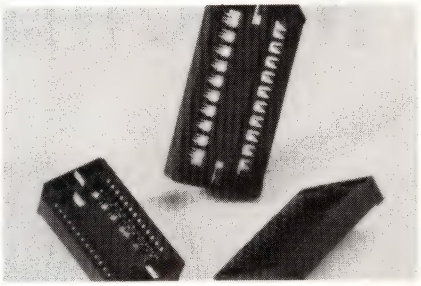
A compact, versatile connector that's certified to ISO 9001 standards offers the function of a fiber-optic and power connector in one device. The Han connector permits combining up to 36 optical fibers with power contacts in many arrangements of 1-mm polymer fiber and 40-A power positions. The tough unit satisfies NEMA 4 enclosure ratings. Fiber-optic contact attenuation is less than 3 dB and wavelength is 660 nm. A standard insert carries up to 108 contacts. Adding a second unit doubles capacity. Call for pricing and delivery.



Harting Elektronik Inc.
2155 Stonington Ave., Suite 212
Hoffman Estates, IL 60195
(708) 519-7700
▶CIRCLE 617

▼ SOCKET HANDLES STATIC AND VIDEO RAM

The latest static RAMs, video RAMs, and 16-Mbit DRAMs can all be socketed using the SOJ Series sockets. Sizes range from 24 to 40 positions with 0.400- and 0.300-in. centerlines. Features include a high-temperature insulator body and compatibility with surface-mount processing equipment. Tape-and-reel and tube-packaging options are available, as are locator posts for hand placement. Pricing ranges from $0.60 to $0.75 in lots of 5000, depending on size.



Augat Inc.
P.O. Box 2510
Attleboro Falls, MA 02763
(508) 699-7646
▶CIRCLE 618

CONNECTOR AND PACKAGING MANUFACTURERS

PCD Inc.
2 Technology Dr.
Peabody, MA 01960
(508) 532-8800
(FC) (CE) (ZI) (MD)
CIRCLE 885

Penstock Inc.
520 Mercury Dr.
Sunnyvale, CA 94086-4018
(408) 730-0300
(RF) (CX) (SM) (CO)
CIRCLE 886

Phoenix Contact Inc.
P.O. Box 4100
Harrisburg, PA 17111-0199
(717) 944-1300
(DS) (DI) (FC) (ID) (SM) (CC)
(PC) (VB) (MB) (BB)
CIRCLE 887

Praegitzer Industries Inc.
9255 S.W. Pioneer Ct.
Wilsonville, OR 97070
(503) 682-5500
(SS) (DD) (ML) (BP) (PC)
(VB) (SB) (MB) (IB) (BU) (GB)
CIRCLE 888

Precision Interconnect
16640 S.W. 72nd Ave.
Portland, OR 97224
(503) 620-9400
(CD) (CO) (TW)
CIRCLE 889

Pyle-National
1334 N. Kostner Ave.
Chicago, IL 60651
(312) 342-6300
(RF) (CX) (EL) (CD) (MD)
(HV) (HC) (RP)
CIRCLE 890

RF Industries Ltd.
7620 Miramar Rd.
San Diego, CA 92126
(619) 549-6340
(PC) (CO)
CIRCLE 891

RIA electronic Inc.
15 Meridian Rd., P.O. Box 447
Eatontown, NJ 07724
(908) 389-1300
(CD)
CIRCLE 892

Radstone Technology Corp.
20 Craig Rd.
Montvale, NJ 07645
(201) 391-2700
(VB) (MI)
CIRCLE 893

Raychem Corp.
300 Constitution Dr.
Menlo Park, CA 94025
(415) 361-3333
(CX) (DS) (FC) (ID) (MD) (CO)
(FL) (TW) (SH) (PW) (HK)
(MG) (ER) (GK) (TB)
CIRCLE 894

Richard Hirschmann of America Inc.
Industrial Row, P.O. Box 229
Riverdale, NJ 07457
(201) 835-5002
(DI) (CD) (HV) (RP)
CIRCLE 895

Rittal Corp.
Electronic Products
One Rittal Pl.
Springfield, OH 45504
(513) 399-0500
(GP) (BM) (CN) (IN)
(VR) (WT) (PT) (EM)
(ER) (VE) (WN)
CIRCLE 896

Rogers Corp.
Microwave/Circuit Materials
P.O. Box 4000
Chandler, AZ 85226
(602) 917-5270
(SS) (DD) (ML) (FX)
CIRCLE 897

Rogers Corp.
Power Distribution
5750 E. McKellips Rd.
Mesa, AZ 85205
(602) 830-3370
(PW) (HN) (BB)
CIRCLE 898

STRONGBOX
P.O. Box 2726
Culver City, CA 90231-2726
(310) 305-8288
(GP) (BM) (IN) (VR)
(EM) (MI)
CIRCLE 903

Samtec Inc.
P.O. Box 1147
810 Progress Blvd.
New Albany, IN 47151-1147
(812) 944-6733
(EL) (FC) (ID) (ZI) (SM) (CC)
(DP) (PG) (CD) (FL)
CIRCLE 899

Schroff Inc.
170 Commerce Dr.
Warwick, RI 02886
(401) 732-3770
(DI) (BP) (VB) (MB)
(BU) (HN) (BB) (GP) (BM)
(CN) (IN) (VR) (PT)
(EM) (ER) (GK)
CIRCLE 900

Siecor Corp.
P.O. Box 489
Hickory, NC 28603-0489
(704) 327-5000
(RP) (FO) (SH) (HN) (GP)
(VR) (WT) (CM)
CIRCLE 901

Specialty Electronics Inc.
629 A Lowther Rd.
Lewisberry, PA 17339
(717) 938-6171
(ID) (SM) (CD) (HN)
CIRCLE 902

Switchcraft Inc.
5555 N. Elston Ave.
Chicago, IL 60630
(312) 792-2700
(AU) (DI) (CD)
CIRCLE 904

Technit Inc.
129 Dermody St.
Cranford, NJ 07016
(201) 272-5500
(ER) (GK) (SE) (TB) (RC)
(VE) (WN)
CIRCLE 905

Technology 80 Inc.
658 Mendelssohn Ave. N.
Minneapolis, MN 55427
(612) 542-9545
(VB) (SB) (MB) (IB) (GB)
CIRCLE 906

Teradyne Inc.
Connection Systems Div.
44 Simon St.
Nashua, NH 03060
(603) 889-5156
(ZI) (SM) (MD) (ML) (WR)
(BP) (PC) (VB) (SB) (MB)
(BU) (BB) (MI) (ER)
CIRCLE 907

Texas Instruments
Connector Systems
34 Forest St.
Attleboro, MA 02703
(508) 699-5213
(PG) (CD) (MD) (BI)
CIRCLE 908

The Bergquist Co.
7705 Bush Lake Rd.
Edina, MN 55439
(612) 835-2322
(PW)
CIRCLE 909

Thomas & Betts Corp.
Electronics Div.
200 Executive Center Dr.
Greenville, SC 29616-2401
(803) 676-2900
(DS) (DI) (FC) (CE)
(ID) (SM) (CC) (DP)
(PG) (CD) (RP) (FO)
CIRCLE 910

Tracewell Enclosures Inc.
567 Enterprise Dr.
Westerville, OH 43081
(614) 846-6175
(BB) (GP) (BM) (IN) (VR) (PT)
(EM) (MI) (CM) (ER) (GK)
CIRCLE 911

Tricon Industries Inc.
Electromechanical Div.
1600 Eisenhower Lane
Suite 200
Lisle, IL 60532-2167
(708) 964-2330
(CD)
CIRCLE 912

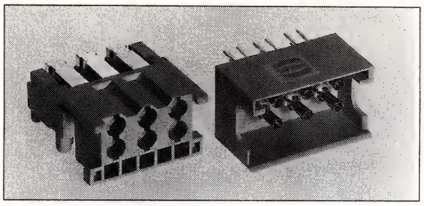
Trompeter Electronics
31186 La Baya Dr.
Westlake Village, CA 91362
(818) 707-2020
(AU) (RF) (CX) (MD)
(HV) (HC) (RP) (CO)
(ES) (MG) (ER)
CIRCLE 913

Tru-Connector Corp.
245 Lynnfield St.
Peabody, MA 01960
(508) 532-0775
(AU) (RF) (CX) (DI)
(CD) (MD) (HV) (RP)
CIRCLE 914

US Conec Ltd.
P.O. Box 2306
Hickory, NC 28603-2308
(704) 323-8883
(FO)
CIRCLE 915

(see p. 136 for key)
(continued on p. 136)

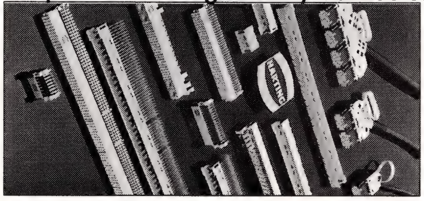
NEW HIGH DENSITY MICRO-COAXIAL CONTACTS



Designed for high speed data transfer rates. Can be used in the IEC 1076-4-2 2.5mm High Density connector system, har-pak®. Provides more space efficiency, high frequency capability, easy handling, low applied cost and application with current equipment practice and emerging metric equipment practices. Designed for PCB termination on both daughtercard to backplane connection; allowing users to bring signal directly into the backplane without a cable transition.

CIRCLE 91

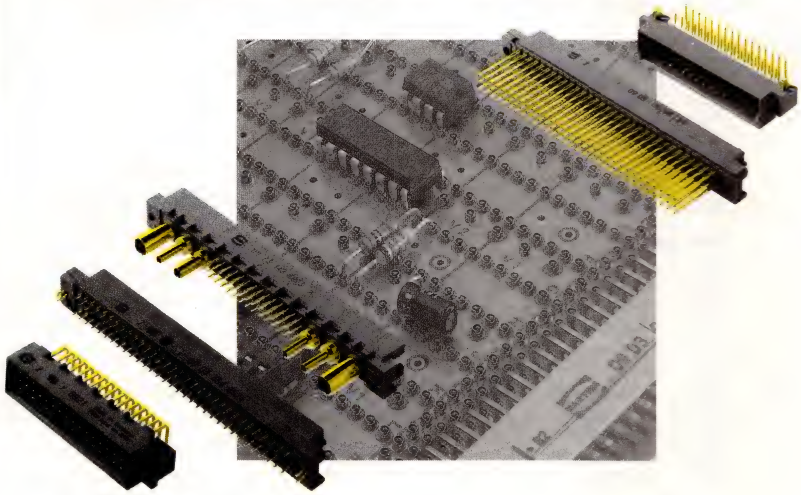
har-pak® 2.5 MM High Density Connector system



Developed for backplane and daughterboard applications in modern rack systems. The 5 row 2.5 mm connector design offers solderless PCB terminations, optimum utilization of space, three dimensional modularity, high contact density, EMI protection, and the ability to double-side surface mount components on daughter cards without loss of a 15 mm card pitch. The har-pak connector system permits using a three dimensional 2.5 mm grid. With the exceptional capabilites of the connector, only one connector style is required to solve your power, signal, ground, and high data rates; simplifying the design and manufacturing of future systems. The compliant pin technology utilizes the same 1 mm plated through hole standard for many DIN 41 612 compliant pin technologies. The consistency in design uses the many years of manufacturing and design experience already available. These attributes combined can lead to new advancements n board-level designs: 15 mm card pitch with double-sided surface mounted daughter cards, butterfly or mid-plane techniques, modular design both horizontally and vertically, low number of system components, combination with other standardized packaging systems, and lower applied costs. **CIRCLE 92**

Gds A DIN connectors

Efficient



HARTING is a hallmark of innovation and reliability worldwide – throughout the electronics industry and in the switchgear sector.

With the Gds A standard DIN 41612 printed circuit connectors, HARTING not only meets top requirements in terms of precision and quality but also makes a contribution to progress in the field of automation. The Gds A connector is mounted and fixed to the PC board in a single procedure. Components, solder pins and the fastening clips of the connector can thus be soldered in a single process.

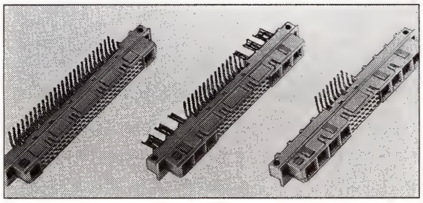
With a comprehensive range of connectors, HARTING offers perfect solutions for all applications.

Connectors from HARTING – the quality connection

HARTING ELEKTRONIK, Inc. · 2155 Stonington Ave. · Suite 212
P. O. Box 95710 Hoffman Estates, Illinois 60195, U.S.A.
Phone 708 / 519 - 7700 · Fax 708 / 519 - 9771

CIRCLE 95

WÄCHTER BREMEN



COMPLIANT PIN DIN 41612-TYPE M INVERSE CONNECTORS

HARTING'S compliant pin Inverse Type M DIN 41612 Eurocard connectors allow-continued development of backplane technology using solderless termination and double-side surface mounting. Applications include telecom, medical and high speed computers. Connector-cavities accommodate the DIN 41626 high voltage, power, coaxial or fiber optic contacts. Connector arrangements can accommodate 2 to 10 special purpose contacts and 78 to 6 standard contacts respectively. Compatible with HARTING male press-in tooling without modification, it can be delivered with special press-in inserts to allow use of 'Flat Rock" or simple flatpress-in dies. **CIRCLE 93**

'har-mik®', NEW MINATURE CONNECTORS FROM HARTING ELEKTRONIK

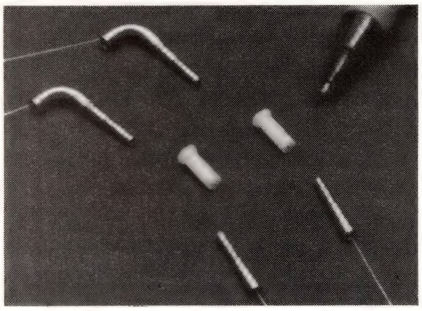
New, comprehensive range of miniature connectors, the 'Pin and Socket' I/0 connectors Series 60.01/02/03/04, are designed to meet the requirements of internal and external connections of the future.

- Reduced size: contact pitch of 1,27 mm
- High contact density: double standard D-Sub
- E.M.I./R.F.I. protected. metal shells and hoods for optimum screening
- Polarized by D shape
- Coding: without contact loss
- Locking device: quick latch for S.C.S.I /RS 232 E applications. Jackscrew for I.P.I/HI.P.P.I applications
- Male and female IDC versions for discrete wire 28 to 30 AWG
- Male and female connectors wth straight and angled solder pins
- Many connector sizes: from 20 to 100 ways

CIRCLE 94

▼ FIBER-OPTIC TERMINUS BOASTS CONSISTENCY

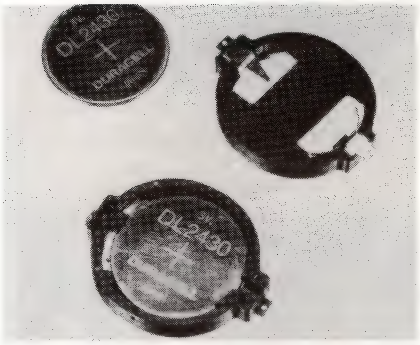
Extremely consistent optical performance over a wide range of environments and service conditions is featured by an expanded-beam fiber-optic terminus system. The model 1087 radiation-hardened terminus system is meant for optical interconnect applications in commercial and military/aerospace applications. Each terminus uses a plano-convex lens to focus and transfer the transmitted light. This produces a collimated beam between termini, resulting in very stable optical performance and little or no degradation. The termini accept 100/14-μm fibers and are adaptable to other sizes. Pricing is $150 in lots of 1000. Delivery is in six to eight weeks.



G&H Technology Inc.
750 W. Ventura Blvd.
Camarillo, CA 93010
(805) 484-0543
▶CIRCLE 619

▼ COIN-CELL HOLDER STANDS 0.177 IN. HIGH

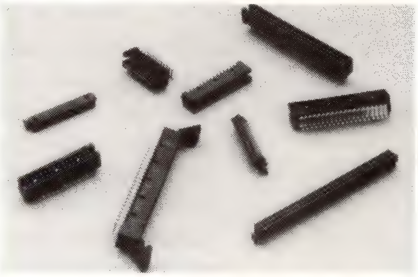
A low-profile, surface-mounted coin-cell battery holder stands just 0.177 in. above the pc board. The unit allows close stacking of pc boards and facilitates the design of compact equipment. Its contacts provide high normal forces, which lock the coin cell firmly into position despite the holder's low height. Contacts are of nickel-plated stainless steel. The holder itself is of high-temperature thermoplastic that suits the IR-reflow process. Seven sizes are offered with samples available on request. Pricing is from $0.50 to $0.95, depending on quantity.



Specialty Electronics Inc.
629A Lowther Rd.
Lewisberry, PA 17339
(803) 457-3824
▶CIRCLE 620

▼ DENSE CONNECTORS BOAST PRECISE CONTACTS

The Advance50 and Advance50SMT connector systems permit 0.050-in.-centerline pc-board packaging. The shrouded receptacles and post-header assemblies incorporate the company's gold-plated HourGlass receptacle contacts, which mate with its Transition Pin. That pin offers a full-radius tip that transitions from a 0.018-in. diameter at the base to a tin-plated solder tail for either through-hole or SMT applications. The system consists of dual-row vertical and horizontal shrouded receptacles and shrouded mating male-post assemblies for perpendicular, parallel, and stacked configurations.



Interconnect Industries Inc.
859 South Rd., Unit 24-102
Wappingers Falls, NY 12590
(914) 227-1147
▶CIRCLE 621

CONNECTOR AND PACKAGING MANUFACTURERS

Unitrack Industries Inc.
967 E. Masten Circle
Milford, DE 19963
(302) 424-5050
(VR)
CIRCLE 916

Vernitron Corp.
Beau Interconnect Div.
P.O. Box 10
Laconia, NH 03246
(603) 524-5101
(CD) (HV) (HC) (RP) (TE)
CIRCLE 917

W.L. Gore & Associates Inc.
Electronic Prods. Div.
555 Paper Mill Rd.
Newark, DE, 19714
(302) 738-4880
(CO) (FL) (TW) (SH)
(PW) (HK) (ER)
CIRCLE 918

Wearnes Hollingsworth Corp.
Electronic Connector Div.
4 Chrysler
Irvine, CA 92718
(714) 855-6404
(FC) (CE) (ID) (CD) (FL) (HN)
CIRCLE 919

XTO Inc.
110 Wrentham Dr.
Liverpool, NY 13088
(315) 451-7807
(ER) (GK) (FR)
CIRCLE 920

Yamaichi Electronics Inc.
1420 Koll Circle, Suite B
San Jose, CA 95112
(408) 452-0797
CIRCLE 921

Zierick Manufacturing
Research & Development
Radio Circle
Mt. Kisco, NY 10549
(914) 666-2911
(AU) (RF) (CX) (ID)
(ZI) (SM) (CD) (RP)
CIRCLE 922

Zoltech Corp.
16658 Arminta St.
Van Nuys, CA 91406
(818) 780-1800
(BP) (VB) (GB) (GP) (BM)
(EM) (CM)
CIRCLE 923

KEY

Connectors and Sockets

(AU)	Audio
(RF)	Radio-frequency
(CX)	Coaxial
(DS)	D-subminiature
(DI)	DIN design
(EL)	Elastomeric
(FC)	Flat cable
(CE)	Card edge
(ID)	Insulation displacement
(ZI)	Zero/low insertion force
(SM)	Surface mountable
(CC)	Chip carriers
(DP)	DIP/SIP
(PG)	Pin-grid array
(CD)	Custom design
(MD)	Military design
(BI)	Test and burn-in
(HV)	High-voltage
(HC)	High-current
(RP)	Rack-and-panel
(FO)	Fiber optic
(TE)	Terminal blocks

Boards and Panels

(SS)	One-sided
(DD)	Double-sided
(ML)	Multilayer
(WR)	Wire-wrap
(FX)	Flexible
(BP)	Backplane
(PC)	Printed circuit
(VB)	VME bus
(SB)	Standard bus
(MB)	Multibus
(IB)	IBM PC bus
(BU)	Futurebus
(GB)	Other bus

Wire and Cable

(CO)	Coaxial
(FL)	Flat
(TW)	Twisted-pair
(SH)	Shielded
(WV)	Woven
(PW)	Power cords/cables
(MN)	Magnet wire
(HK)	Hookup wire
(HN)	Harnesses
(CA)	Cabling materials
(BB)	Bus bars

Enclosures

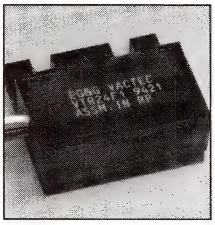
(GP)	General purpose
(BM)	Bench-mounted
(CN)	Consoles
(IN)	Instrument cases
(VR)	Vertical racks
(WT)	Water-tight
(PT)	Portable
(EM)	EMI/RFI design
(MI)	Military design
(CM)	Custom design

Shielding

(ES)	Electrostatic
(MG)	Magnetic
(ER)	EMI/RFI
(GK)	Gasket
(FR)	Ferrites
(SE)	Sheets/strips
(TB)	Tubing
(RC)	Rooms and chambers
(VE)	Vents
(WN)	Windows

▼ LONG RANGE SENSING IN MATCHBOX SIZE

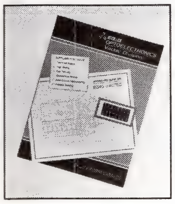
Ideal for applications requiring object sensing and material control. The VTR24F1 retro-reflective optical switch extends the range of contactless, optical position sensing. Almost the size of a matchbox, it senses objects up to 4 inches. Designed to "see" almost any surface including matte, gloss, or black, this sensor provides a switchlike response, low position error, and CMOS compatibility.



EG&G Optoelectronics
Vactec Division
10900 Page, St. Louis, MO 63132
Phone (314) 423-4900
Fax: (314) 423-3956
READER SERVICE 187

▼ NEW SHORT-FORM CATALOG

A new short form catalog depicting a complete line of optoelectronic components is now available from EG & G Optoelectronics, Vactec Division.

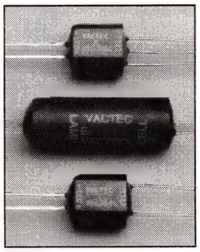


Included in this concise, 12-page catalog are electrical/optical characteristics, features, and typical applications for EG & G Vactec's complete line of silicon photodiodes; IR emitters and phototransistors; Cds photoconductive cells; analog optoisolators (Vactrols®); and optoswitches, optical hybrids, and custom opto assemblies. For free copies, please contact:

EG&G Optoelectronics
Vactec Division
10900 Page, St. Louis, MO 63132
Phone (314) 423-4900
Fax: (314) 423-3956
READER SERVICE 188

▼ IDEAL FOR AUDIO APPLICATIONS

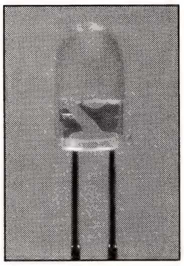
Analog Optoisolators (Vactrols™) are ideal as power limiters and remote gain control in audio amplifiers. Used widely in professional and automobile audio equipment, Vactrols™ provide low noise and low harmonic distortion making them ideal for use as electronically adjusted variable resistors. The Vactrols™ catalog discusses audio applications such as gating, muting, limiters, AGC distortion, and switching.



EG&G Optoelectronics
Vactec Division
10900 Page, St. Louis, MO 63132
Phone (314) 423-4900
Fax: (314) 423-3956
READER SERVICE 189

▼ OPTIMIZED OPTICS

The VTE1285 high output IR Emitting Diode (IRED) incorporates an aspheric lens to optimize the amount of power focused into its output beam. This 5 mm diameter plastic package contains a 880 nm high efficiency IRED chip. Typical power output at 100 mA drive is 20 mW. Typical total half power beam angle is 16 degrees. A companion part, the VTE1295 is U.L. Component recognized. Applications include smoke detectors, remote controls, and security systems.



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Vactec Division
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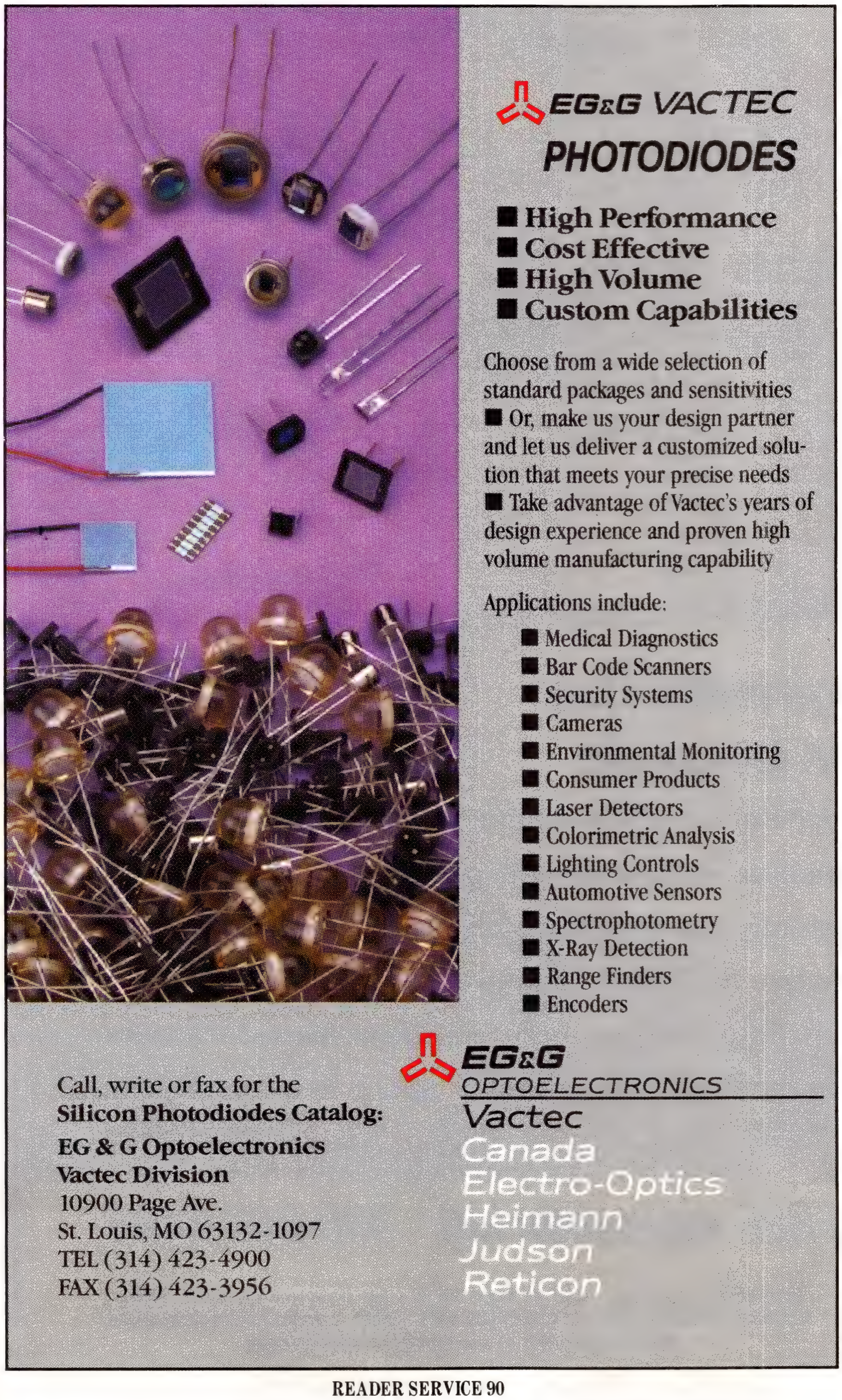

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- ■ Spectrophotometry
- ■ X-Ray Detection
- ■ Range Finders
- ■ Encoders

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READER SERVICE 90

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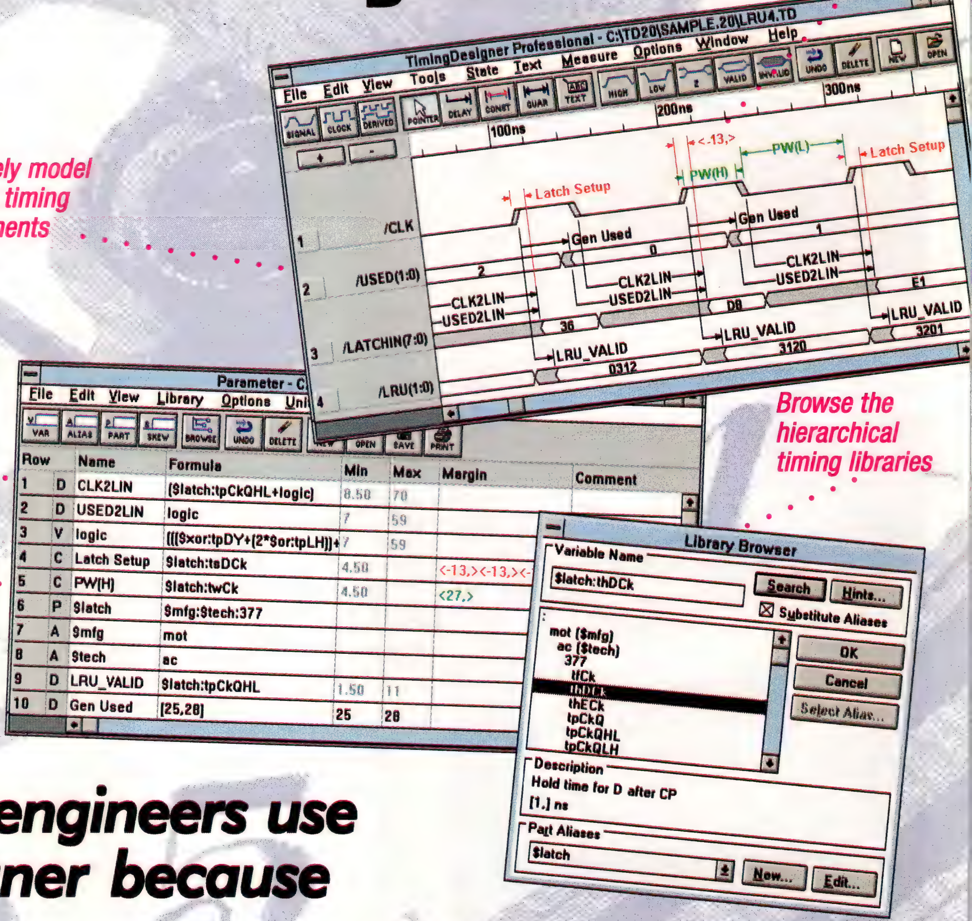

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Row		Name	Formula	Min	Max	Margin	Comment
1	D	CLK2LIN	($latch:tpCkQHL+logic)	8.50	70		
2	D	USED2LIN	logic	7	59		
3	V	logic	((($xor:tpDY+(2*$or:tpLH))+	7	59		
4	C	Latch Setup	$latch:tsDCk	4.50		<-13,><-13,><-	
5	C	PW(H)	$latch:twCk	4.50		<27,>	
6	P	$latch	$mfg:$tech:377				
7	A	$mfg	mot				
8	A	$tech	ac				
9	D	LRU_VALID	$latch:tpCkQHL	1.50	11		
10	D	Gen Used	[25,28]	25	28		

Variable Name: $latch:thDCk

☒ Substitute Aliases

:
mot ($mfg)
ac ($tech)
377
tfCk
thDCk
thECk
tpCkQ
tpCkQHL
tpCkQLH

Description: Hold time for D after CP
[1.] ns

Part Aliases: $latch

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- the **best** way to visualize timing relationships in complex clock trees
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READER SERVICE 153

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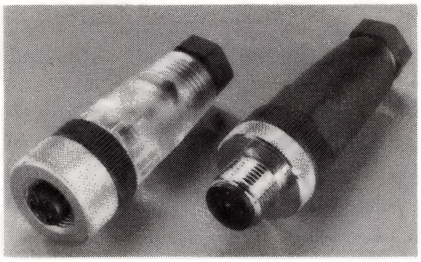
Telephone (206) 869-4227 FAX (206) 869-4229 EMAIL chronco!sales@uunet.uu.net
FAX us for a list of our European distributors

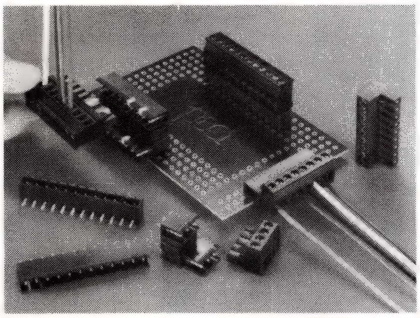
▼ 12-MM ROUND CONNECTORS BOOST SENSOR OPTIONS

Unlike most micro-connectors, which are produced only as pre-molded assemblies, the E-Series of 12-mm circular connectors can be wired in the field. Users can easily adapt valves, actuators, proximity switches, and hard-wired sensing devices to the micro ports provided on many junction boxes. The connectors also enable easy retrofitting and/or repair of existing sensors and actuators, as well as conversion of any hard-wired device into a quick-disconnect unit. The units are offered as female receptacles or male plugs in straight and right-angle versions and with four or five poles. Pricing for a four-pole, straight plug unit is $6.01 in small lots. Delivery is from stock to six weeks.



Richard Hirschmann Of America Inc.
Industrial Row
P.O. Box 229
Riverdale, NJ 07457
(800) 225-0524, ext. 230
▶ **CIRCLE 633**

▼ TERMINAL BLOCKS GAIN ENHANCEMENTS

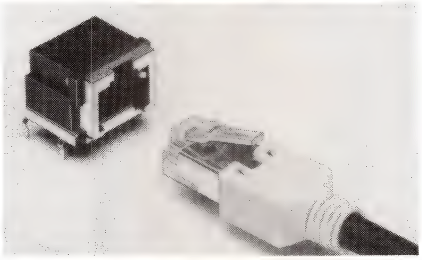


Significant expansion of the application range and flexibility of the ELF family of 0.200-in./5-mm spacing pluggable terminal blocks and headers has been achieved. The plugs and headers, which are designed for reliable board-to-wire connections, now come with selective gold plating on contacts for critical applications in low-level circuits or severe environments. Plating is 0.000030 in. gold over 0.000050 in. nickel. Integrally molded locking ears are also offered for all devices. The ears capture a floating, slot-head locking screw which engages a threaded insert on the header ear and tightens to firmly secure the connector after mating. Pricing for a 10-position plug and header with keying starts at $4.50 in lots of 1000. Delivery is in two weeks.

PCD Inc.
Two Technology Dr.
Peabody, MA 01960
(508) 532-8800
▶ **CIRCLE 634**

▼ MODULAR CONNECTORS PROVIDE EMI SHIELDING

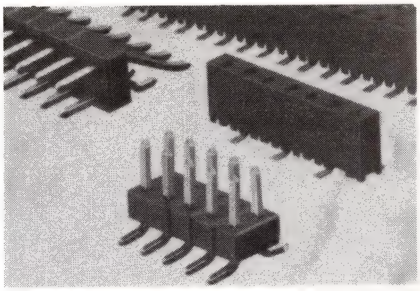
A line of TM11 modular connectors is available with EMI-shielding protection. The one-piece construction of the shell and clamp offers excellent shielding for ISDN terminals and PCs, LAN boards, and the data-communication industry. The jack is built to allow the shielding to easily engage and lock first upon mating. A metal shell offers ESD protection and a plastic cover is provided for enhanced aesthetics. Available in either six or eight positions, the TM11 connector replaces the RJ45 connector. Pricing in lots of 10,000 is $1.25 for plugs and from $1.75 to $3.25 for shielded jacks, depending on options.



Hirose Electric (U.S.A.) Inc.
2688 Westhills Ct.
Simi Valley, CA 93065
(805) 522-7958
▶ **CIRCLE 635**

▼ 2-MM SMT CONNECTORS NOW INCLUDE STRIPS

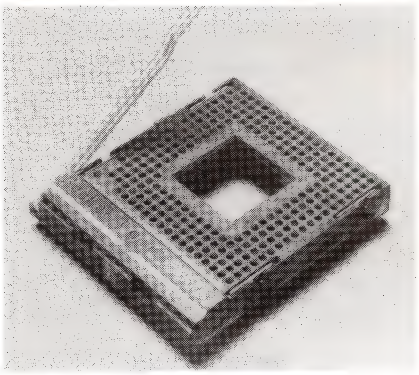
New sockets and terminal strips have been added to Samtec's line of 2-mm surface-mount interconnects. The MMS Series socket strips stand 0.175 in. tall and feature double-beam phosphor bronze contacts. They come in four styles: single- and double-row with vertical and horizontal mounting. The MMT Series terminal strips come in the same four styles for mating with the MMS and other Samtec SMT 2-mm socket strips. Mated height for the pair is 7.44 mm (0.293 in.). Cost is from $0.05 per position for the MMS Series and from $0.047 per position for the MMT Series. Delivery is in five days from receipt of order.



Samtec Inc.
P.O. Box 1147
New Albany, IN 47151-1147
(800) SAMTEC-9
▶ **CIRCLE 636**

▼ INTEL QUALIFIES PGA ZIF SOCKET

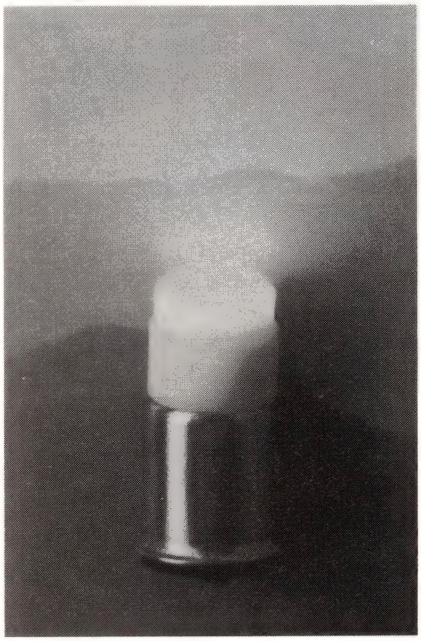
A 236-pin PGA ZIF socket from Aries has been qualified by Intel Corp. for use in PCs that are upgradeable with OverDrive processors. The IS3PGAZIF-236 socket has been rated under extreme environmental conditions to more than 20,000 insertion cycles. In addition to the Intel design, Aries can furnish this socket with variations and options to meet special requirements. These include custom handle configurations and a hinged flap mechanism which prevents users from trying to insert a processor into a closed socket. Pricing for the Intel-approved version is $4.95 in lots of 10,000.



Aries Electronics Inc.
P.O. Box 130
Frenchtown, NJ 08825
(908) 996-6841
▶ **CIRCLE 637**

▼ SIX-CHIP AMBER LED USES BRIGHT AlInGaP

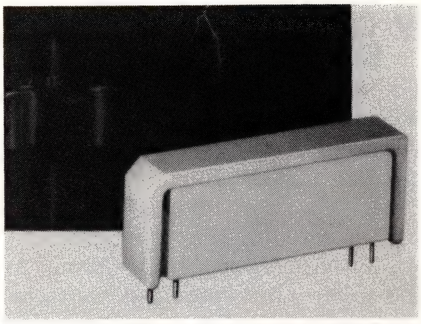
Claimed as the brightest amber multi-chip LED available, the MF200-EA28-6 device is designed to replace the industry-standard 387 incandescent bulb. The LED is based on newly developed AlInGaP chip material with very high luminous efficiency for high light output over a wide voltage range. The unit is designed to operate continuously for upwards of 100,000 hours at 28 V dc while drawing only 14 mA. At 200 mcd, it's much brighter than higher-rated single-chip AlInGaP LEDs, because the six-chip configuration emits greater volume of light over a 160° viewing angle for enhanced peripheral viewing. Pricing in lots of 1000 is $8.60. Delivery is in four to six weeks.



Data Display Products
445 S. Douglas St.
El Segundo, CA 90245-4630
(310) 640-0442
▶CIRCLE 638

▼ LINE-CARD PROTECTORS MELD RESISTOR, FUSE

A resistive device is specifically designed to meet the demanding requirements of Bellcore's TR-1089 spec for circuit protection in telecommunication line cards at resistance values as low as 5.6 Ω. The ALFR line-feed resistor is a combination precision resistor and thermal fuse that protects against both lightning and power-cross conditions. Rated at 2 W, the device offers resistance values from 5.6 to 100 Ω in tolerances to 1%. The four-lead, in-line ceramic package is compatible with automatic insertion. Pricing is $1.60 in lots of 10,000.



IRC Inc.
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(704) 264-8861
▶CIRCLE 639

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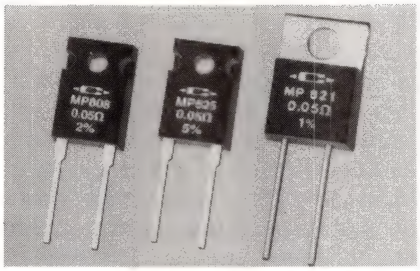
▼ ALUMINUM ELECTROLYTICS BOAST LONG LIFESPAN

Designed specifically for the long life demanded by applications such as uninterruptable power supplies, motor-speed drivers, high-wattage power supplies, and inverters, the CGL aluminum electrolytic capacitor is rated for 2500 hours and up to 450 V dc. The large-can, computer-grade device will be available in a 500-V dc version by the end of 1994. Call for pricing and delivery.

Aerovox Aero M
370 Faunce Corner Rd.
N. Dartmouth, MA 02747-1217
(508) 995-8000
▶ CIRCLE 640

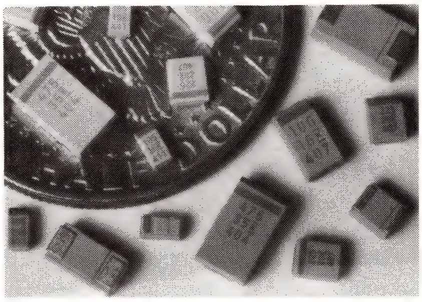
▼ CURRENT-SENSE RESISTORS OFFER VALUES TO 0.05 Ω



With values as low as 0.05 Ω, the MP808, MP825, and MP821 power film resistors are well-suited for power current-sensing applications. The MP808 comes in a TO-126-style power package and dissipates 8 W at a case temperature of 25°C. Values range to 10 kΩ. The MP825 also comes in the TO-126 package and dissipates 25 W at 25°C. The MP821 comes in a TO-220 package with a metal mounting tab and dissipates 20 W. It offers values up to 9.99 Ω. All come in tolerances of ±1, ±2, ±5, ±10, and ±20%. Pricing starts at $1.11 for the MP808 in lots of 10,000.

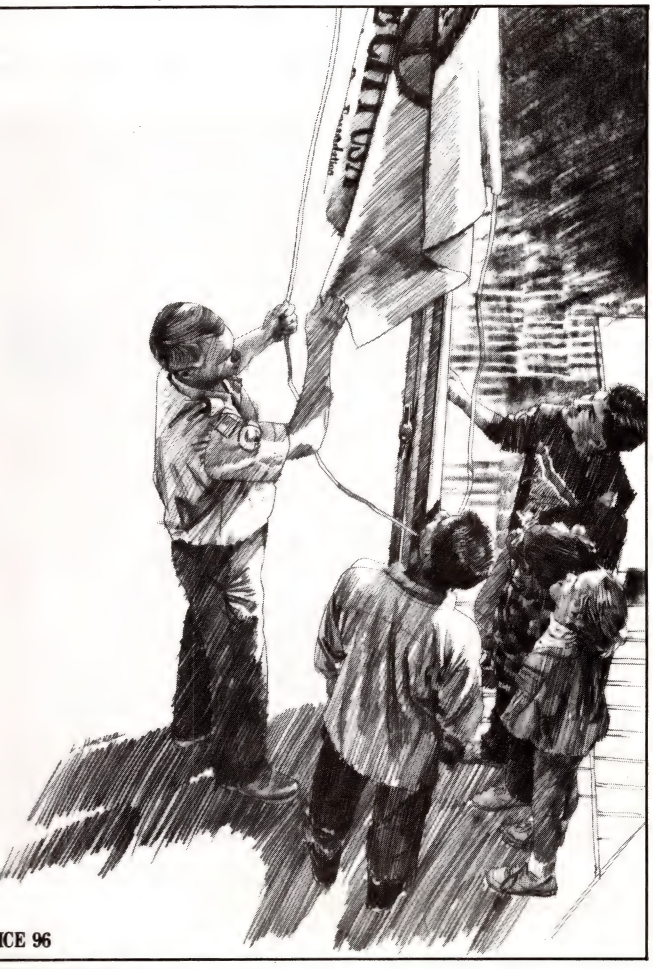
Caddock Electronics Inc.
17271 N. Umpqua Hwy.
Roseburg, OR 97470
(503) 496-0700
▶ CIRCLE 641

▼ TANTALUM CAPACITORS SUIT SURFACE MOUNTING



Lower impedance and higher capacitance is offered in less volume than can-style aluminum electrolytic capacitors designed for surface mounting by the Type TCS tantalum electrolytics. Available in the full range of industry-standard ratings and case sizes, the capacitors boast a wide range of values, high performance over temperature and frequency, and excellent solderability. Values range from 0.1 to 150 μF in voltages from 4 to 50 V dc. Pricing is from $0.095 in lots of 1000. Delivery is from stock to 12 weeks.

Cornell Dubilier
1605 E. Rodney French Blvd.
New Bedford, MA 02744
(508) 996-8564
▶ CIRCLE 642



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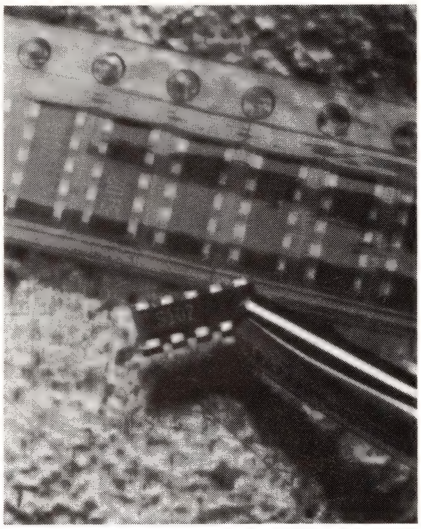
The National Arbor Day Foundation™

READER SERVICE 96

▼ CERAMIC R NETWORKS CURTAIL FLEX WOES

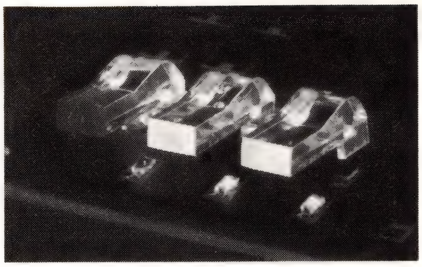
A line of ultra-small ceramic chip resistor networks is well suited for use in notebook and palmtop computers. The bussed MNR-35 networks sidestep reliability problems found in such applications with traditional molded resistor networks being attached to flexible circuit boards. Each network features eight resistive elements with two electrodes positioned in common. The devices may be supplied with one- and six-pin common or 5- and 10-pin common connections. The eight resistors make the networks especially useful in digital applications such as pull-up or pull-down circuits. The 0.063-W devices range from 100 Ω to 100 kΩ. Pricing is $0.12 in small quantities with delivery in 10 weeks.



Rohm Corp.
3034 Owen Dr.
Antioch, TN 37013
(615) 641-2020, ext. 116
▶ CIRCLE 643

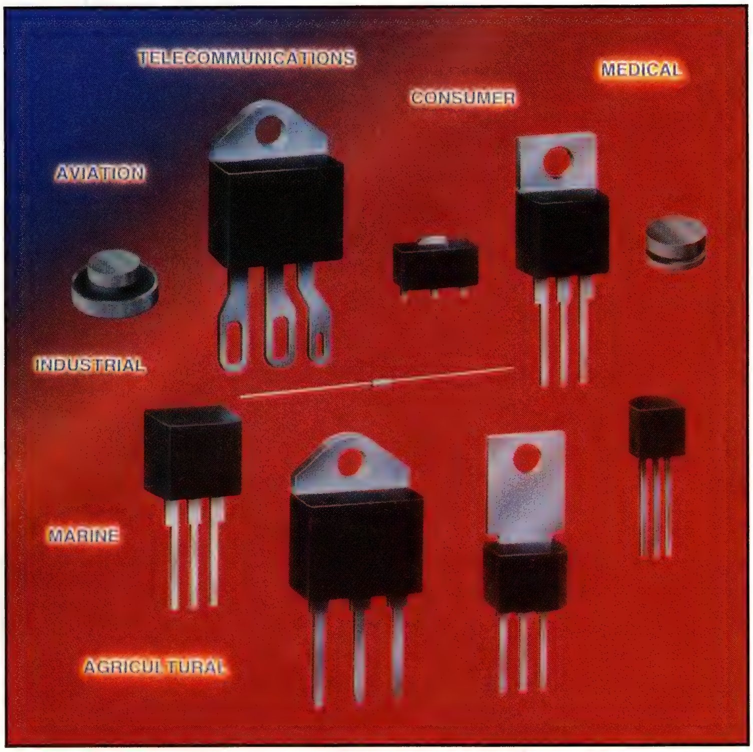
▼ LED LIGHT PIPES ROUTE OUTPUT TO PANEL

Light from LEDs is routed from its source to the intended viewing location by a family of light pipes from Dialight. The pipes complement the microLED Series of LEDs. The precision-molded plastic components are attached to the circuit board or front panel after soldering. Typically, they route light at a right angle from the pc board. They're especially useful in applications requiring a horizontal or vertical array of indicators. Products in the family range from round 3- and 5-mm illuminating surfaces to multiple-height squares, and a light pipe that mounts over an RJ45 jack for LAN applications. Prices start at $0.59 in lots of 1000. Samples are available now and production deliveries take from four to six weeks.



Dialight Corp.
Dept. P-MLP
1913 Atlantic Ave.
Manasquan, NJ 08736
(908) 223-9400
▶ CIRCLE 644

Custom Thyristors For Tough Applications



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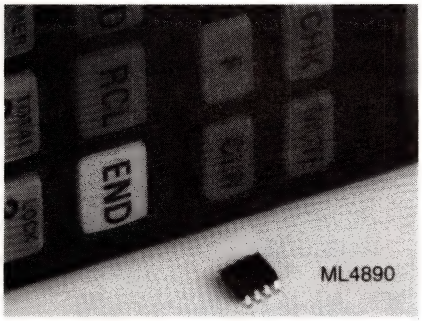
READER SERVICE 131

▼ DC-DC-CONVERTER CHIP POWERS CELLULAR PHONES

A single alkaline battery is all that's needed to power noise-sensitive handheld products such as cellular phones, pagers, and medical instruments when they contain the ML4890 dc-dc-converter IC. The chip also works with single-cell lithium, nickel metal hydride, or nickel cadmium batteries. The device boosts battery voltages as low as 0.9 V into either 5, 3.3, or 3 V with virtually no output ripple (2 mV p-p). A second version can be configured to produce any voltage from 2 to 5.5 V. Pricing for the 8-pin SOIC is $2.95 in lots of 1000. Samples available now; full production slated for September.



Micro Linear Corp.
2092 Concourse Dr.
San Jose, CA 95131
(408) 433-5200
▶ CIRCLE 645

▼ PCMCIA REGULATORS POWER, GUARD VPP PINS

Thanks to built-in current limiting and thermal shutdown, the LT1312 single and LT1313 dual PCMCIA regulators ensure that a short circuit on either side of a standard PCMCIA socket will not damage the host computer or PCMCIA card through the VPP pins. Further, the devices produce clean, tightly regulated outputs of zero, 3.3, 5, and 12 V from any available unregulated 13-to-20-V supply. This eliminates the cost of an extra 12-V regulator to generate clean VPP power. Direct connection with PCMCIA-interface controllers is provided by means of compatible digital inputs. Pricing in lots of 1000 is $2.03 for the single device and $3.03 for the dual version.

Linear Technology Corp.
1630 McCarthy Blvd.
Milpitas, CA 95035-7487
(800) 454-6327
▶ CIRCLE 646

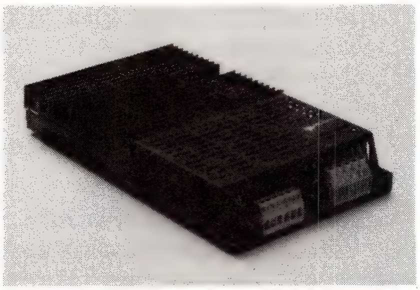
▼ SINGLE-PHASE AC SOURCE CORRECTS POWER FACTOR

The most stringent requirements of the European Community are met by the model BL1350-pf, a power-factor-corrected, single-phase ac-power source with universal input. The unit offers an input power factor of 0.98 as opposed to the 0.65 power factor common to most similar units. For typical ac sources, the input-current waveform shows zero current being drawn for most of the cycle and two sharp surges or spikes at 90° and 270°. The BL1350-pf source completely eliminates these surges and produces an input-current waveform that's a smooth, continuous sine wave. Call for pricing and delivery.

Behlman Electronics Inc.
An Astrosystems Co.
6 Nevada Dr.
Lake Success, NY 11042
(516) 328-1600
▶ CIRCLE 647

▼ AC-DC SWITCHERS OFFER AUTORANGING

An autoranging input, a module-disable feature, and EMI/RFI levels that meet VDE/FCC Class B ratings are among the enhancements that have been made to the FlatPAC family of user-definable ac-dc supplies. These off-line units combine up to three of the company's VI-200 dc-dc converters and front-end assemblies in a set of modular chassis-mount enclosures for systems requring from 50 to 600 W of total output power. The package measures 1.37 in. high by 8.6 in. long in widths of 2.5, 4.9, and 7.4 in. Each internal converter offers one output, 50 to 200 W of output power, and an output voltage from 1 to 95 V dc. In OEM lots, pricing is from $0.85/W.



Vicor Corp.
23 Frontage Rd.
Andover, MA 01810
(800) 735-6200
▶ CIRCLE 648

PICO

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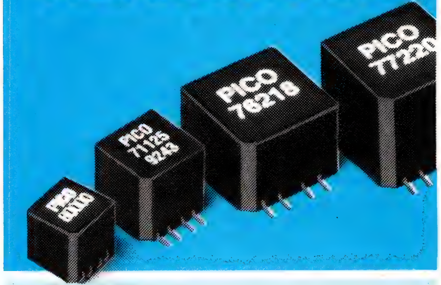
Surface Mount Audio Transformers



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.2" Ht.

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FAX **914-699-5565**

PICO Electronics, Inc.
453 N. MacQuesten Pkwy., Mt. Vernon, N.Y. 10552

READER SERVICE 162

POWER SOURCES

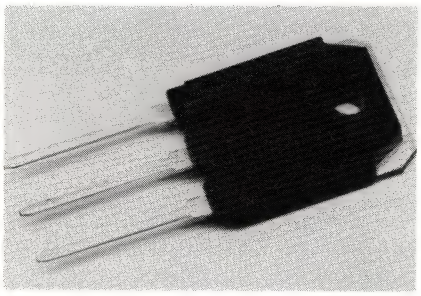
▼ HIGH-POWER DC SUPPLIES MEET VARIED LAB NEEDS

The XHR Series of high-power dc supplies comes in 600- and 1000-W versions to meet the requirements of design engineering, manufacturing test, educational facilities, and research labs. The units are portable enough to fit in the same rack space as a half-rack multimeter. Standard features include programmable dc output, power-factor correction, optional internal GPIB or RS-232 programming, and front and rear input connectors. Call for pricing and delivery.

Xantrex Technology Inc.
8587 Baxter Pl.
Burnaby, B.C., Canada V5A 4V7
(604) 421-3031
▶ CIRCLE 649

▼ FAST-RECOVERY SNUBBERS WITHSTAND LARGE SURGES

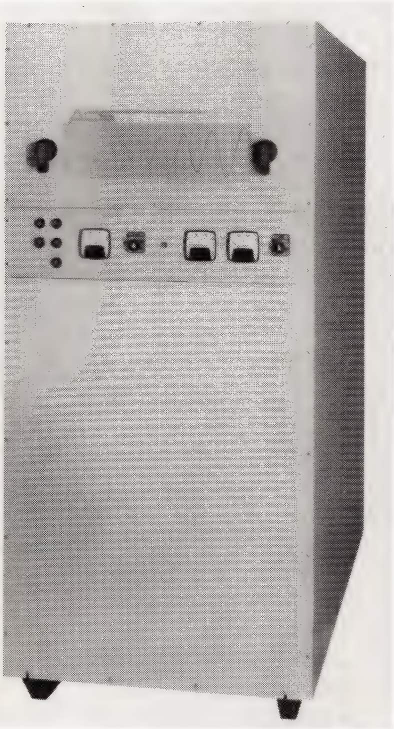
Specifically designed for use in snubber circuits, the RM25HG-24S and RM50HG-12S snubber diodes in TO-3P packages are very fast-recovery types that withstand large surge currents for short durations. The 1200-V rating of the RM25HG-24S makes it particularly useful with the company's 1200-V family of IGBTs and intelligent-power modules. Users can parallel multiples of the device and use it as a compact snubber for IGBTs to 1200 V and 600 A. Typical pricing for the RM25HG-24S is $14.68 in lots of 100. Prototype quantities are available from stock to six weeks.



Powerex Inc.
200 Hillis St.
Youngwood, PA 15697
(800) 451-1415
▶ CIRCLE 650

▼ 50-Hz POWER SOURCE TESTS EXPORT EQUIPMENT

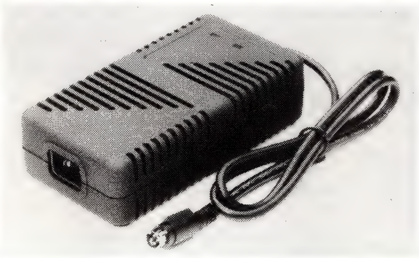
A 125-kVA frequency converter provides a true sine-wave output with high input-to-output isolation for 50-Hz testing of equipment for export to overseas markets. The AFC1 converter withstands system load faults to clear while maintaining output continuity to the remaining load. Ride-through capability is also provided, maintaining output power to the load even during input-power sags and short-term outages. Product offerings range from 500 VA to 200 kVA in all common input and output voltage and phase combinations. A 100-kVA unit goes for $18,595, depending on configuration. Delivery is in six to eight weeks.



Advanced Control Systems
605 E. Alton Ave., Suite A
Santa Ana, CA 92705
(714) 540-9010
▶ CIRCLE 651

▼ EXTERNAL SWITCHERS OFFER CHARGER OPTION

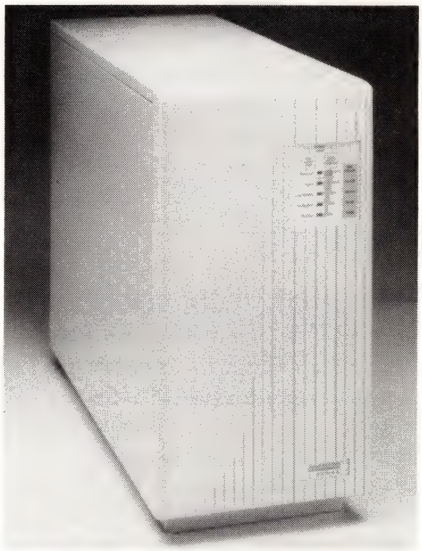
The CL family of 25- and 40-W ac-dc switching power supplies features universal inputs from 90 to 264 V ac at 47 to 440 Hz. Single-, dual-, and triple-output versions offer outputs of ±5, ±12, 9.5, 24, and 48 V dc. Single-output versions of the 25-W model can be had with an optional high-speed, internal, dual-state NiCd battery-charging circuit. The circuit provides 1.2 A of charging current for up to eight cells. All supplies meet FCC and VDE level B line-conducted emissions requirements. Typical pricing is from $35 to $40 for the 25-W models and $55 for the 40-W versions in OEM lots.



Computer Products
Power Conversion America
7 Elkins St.
South Boston, MA 02127
(617) 268-1170
▶ CIRCLE 652

▼ LINE-INTERACTIVE UPS PROTECTS EQUIPMENT

Power instabilities that can damage sensitive equipment are held off by the OnGuard LI-2400 uninterruptible power source (UPS). The unit functions as an intelligent power-protection device, surge suppressor, and power-backup system. Targeted at larger electronic devices, network servers, and midrange systems, the UPS delivers twice the power protection of other units in the LI series. In the event of a power disruption, overload, or short, the system automatically invokes a user-programmable, orderly shutdown of the system or network to preserve its data. Pricing is $1999.



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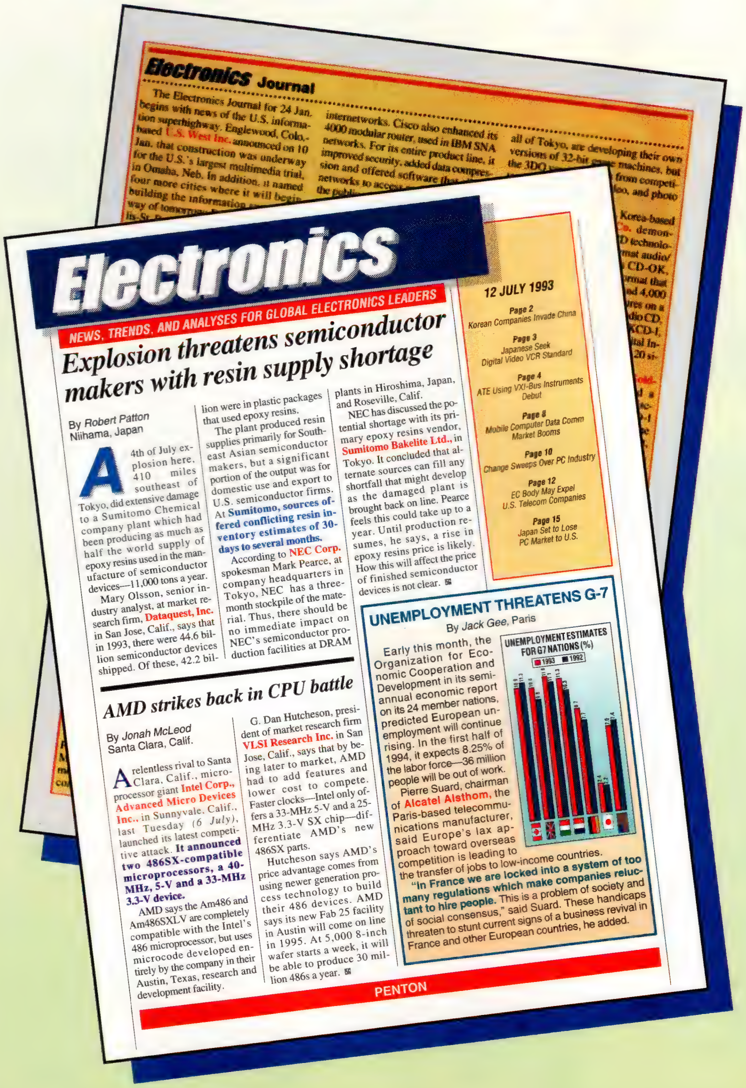

Electronics Journal

The Electronics Journal for 24 Jan. begins with news of the U.S. information superhighway. Englewood, Colo.-based U.S. West Inc. announced on 10 Jan. that construction was underway for the U.S.'s largest multimedia trial, in Omaha, Neb. In addition, it named four more cities where it will begin building the information

Electronics

NEWS, TRENDS, AND ANALYSES FOR GLOBAL ELECTRONICS LEADERS

12 JULY 1993

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Page 15 *Japan Set to Lose PC Market to U.S.*

Explosion threatens semiconductor makers with resin supply shortage

By *Robert Patton*
Niihama, Japan

A 4th of July explosion here, 410 miles southeast of Tokyo, did extensive damage to a Sumitomo Chemical company plant which had been producing as much as half the world supply of epoxy resins used in the manufacture of semiconductor devices—11,000 tons a year.

Mary Olsson, senior industry analyst, at market research firm, **Dataquest, Inc.** in San Jose, Calif., says that in 1993, there were 44.6 billion semiconductor devices shipped. Of these, 42.2 billion were in plastic packages that used epoxy resins.

The plant produced resin supplies primarily for Southeast Asian semiconductor makers, but a significant portion of the output was for domestic use and export to U.S. semiconductor firms. At **Sumitomo, sources offered conflicting resin inventory estimates of 30-days to several months.**

According to **NEC Corp.** spokesman Mark Pearce, at company headquarters in Tokyo, NEC has a three-month stockpile of the material. Thus, there should be no immediate impact on NEC's semiconductor production facilities at DRAM plants in Hiroshima, Japan, and Roseville, Calif.

NEC has discussed the potential shortage with its primary epoxy resins vendor, **Sumitomo Bakelite Ltd.,** in Tokyo. It concluded that alternate sources can fill any shortfall that might develop as the damaged plant is brought back on line. Pearce feels this could take up to a year. Until production resumes, he says, a rise in epoxy resins price is likely. How this will affect the price of finished semiconductor devices is not clear.

AMD strikes back in CPU battle

By *Jonah McLeod*
Santa Clara, Calif.

A relentless rival to Santa Clara, Calif., microprocessor giant **Intel Corp., Advanced Micro Devices Inc.,** in Sunnyvale, Calif., last Tuesday *(6 July)*, launched its latest competitive attack. **It announced two 486SX-compatible microprocessors, a 40-MHz, 5-V and a 33-MHz 3.3-V device.**

AMD says the Am486 and Am486SXLV are completely compatible with the Intel's 486 microprocessor, but uses microcode developed entirely by the company in their Austin, Texas, research and development facility.

G. Dan Hutcheson, president of market research firm **VLSI Research Inc.** in San Jose, Calif., says that by being later to market, AMD had to add features and lower cost to compete. Faster clocks—Intel only offers a 33-MHz 5-V and a 25-MHz 3.3-V SX chip—differentiate AMD's new 486SX parts.

Hutcheson says AMD's price advantage comes from using newer generation process technology to build their 486 devices. AMD says its new Fab 25 facility in Austin will come on line in 1995. At 5,000 8-inch wafer starts a week, it will be able to produce 30 million 486s a year.

UNEMPLOYMENT THREATENS G-7

By *Jack Gee*, Paris

Early this month, the Organization for Economic Cooperation and Development in its semiannual economic report on its 24 member nations, predicted European unemployment will continue rising. In the first half of 1994, it expects 8.25% of the labor force—36 million people will be out of work.

Pierre Suard, chairman of **Alcatel Alsthom,** the Paris-based telecommunications manufacturer, said Europe's lax approach toward overseas competition is leading to the transfer of jobs to low-income countries.

"In France we are locked into a system of too many regulations which make companies reluctant to hire people. This is a problem of society and of social consensus," said Suard. These handicaps threaten to stunt current signs of a business revival in France and other European countries, he added.

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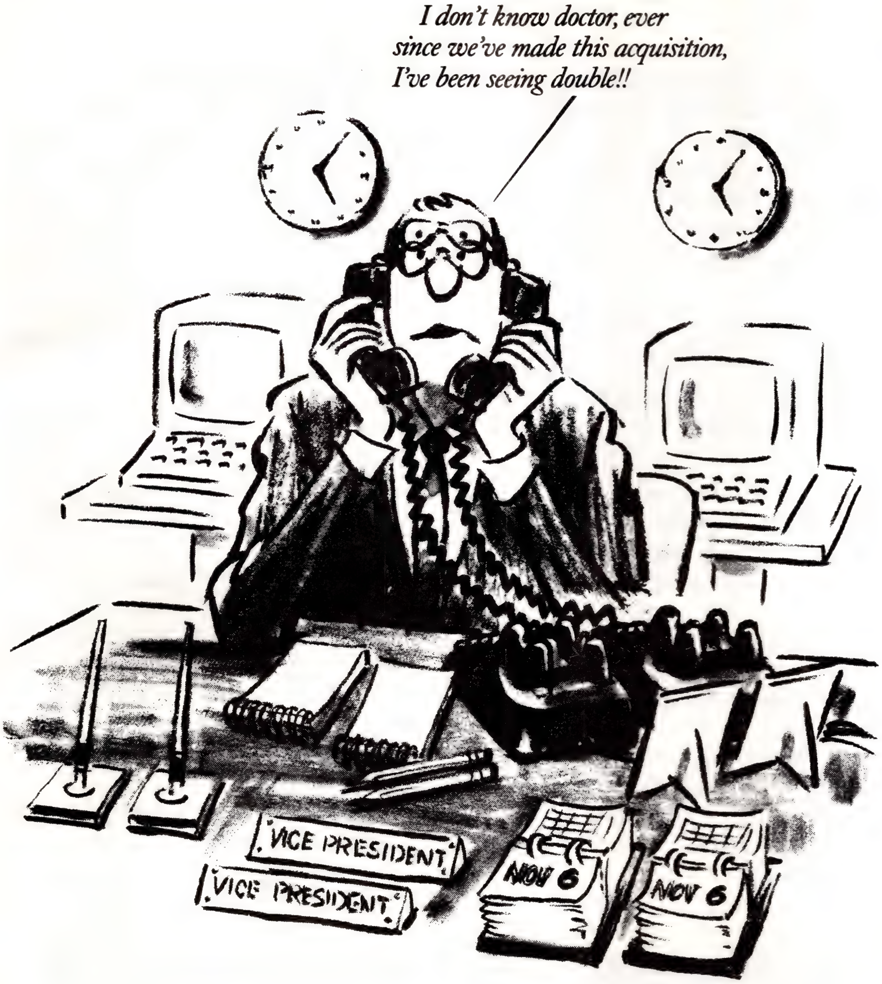
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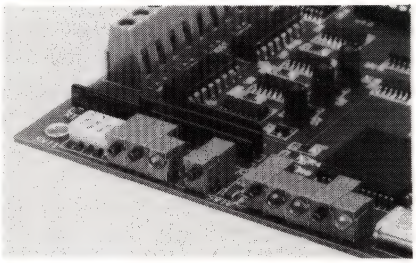
SWITCHES & RELAYS

▼ LEDs AND SWITCHES STACK ON PCB EDGE

Companion LED indicator lamps interlock with miniature, SPDT push-buttons to create status/reset stations at the edge of a pc board. The Series 32 switches and lamps can be had in any arrangement. Red, yellow, and green LEDs are available to complement the switches. Applications include telecom, security, assembly equipment, and instrumentation in which operation must be monitored. The Series 32 devices maintain 0.200 in. between centers of lamps and switch buttons. The assembly measures only 0.272 in. off the board and is 0.400 in. deep. Pricing for the switches is $1 in lots of 1000. The LEDs and their sockets go for $0.39 in lots of 1000.



Grayhill Inc.
561 Hillgrove Ave.
La Grange, IL 60525
(708) 482-2132
▶CIRCLE 654

▼ RELAYS SEAL OUT ALL CONTAMINANTS

A substantial increase in relay life has been secured for the CDR10 and CDR40 relays when used in contaminated atmospheres or with immersion cleaning. Optional epoxy sealing enables the units to withstand corrosive environments. Operation is for more than 100,000 cycles in any industrial environment. Type CDR10, a general-purpose relay, comes in double-pole, double-throw and four-pole, double-throw configurations. It handles up to 5 A for 28-V dc and 240 V ac loads. The CDR40 ups the current handling to 10 A. Pricing in lots of 1000 is $2.70 for the CDR10 and $2.40 for the CDR40. Delivery is from stock to 14 weeks.

Cornell Dubilier
2314 M.L. King Ave.
P.O. Box 2768
Calexico, CA 92231-2768
(619) 357-3441
▶CIRCLE 655

DIP SWITCHES OFFER PACKAGING OPTIONS

Grayhill now offers tape-and-reel packaging for their surface-mount-style rotary DIP switches. The Series 94 switches come with J-bend or gull-wing terminal forms. Thanks to high-temperature plastics, the Series 94 parts can withstand assembly temperatures of up to 260°C. Each switch measures just 0.2 in. above the board. In addition, the switches are internally sealed, eliminating the need for an external tape. Through-hole styles are also available with flush or extended actuators in a perpendicular or right-angle mount. The surface-mount Series 94 cost $1.39 each in 1000-piece lots. They are offered in standard reels containing 750 pieces, and also in tube packaging. Delivery is in 2 to 4 weeks.

Grayhill Inc.
561 Hillgrove Ave.
P.O. Box 10373
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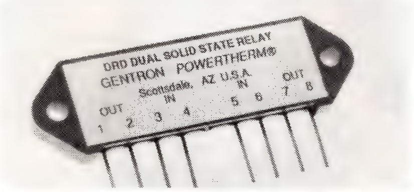
(708) 482-2132
▶CIRCLE 656

SOLID-STATE RELAYS HANDLE LOTS OF POWER



Although tiny in size, the DRD Series ac solid-state relays can control large amounts of power with a low-level dc logic input signal. The relays come in a 2.5-by-0.75-by-0.2-in. package, and are rated for 10 A at 600 V. A triac design provides full-wave control and high-current capability with high dV/dt capability. Zero-cross circuitry switches on at zero voltage and off at zero current for inductive loads. Non-zero-crossing drive circuitry allows for phase and on-off control.

Gentron Corp.
7345 E. Acoma, Suite 101
Scottsdale, AZ 85260
(800) 436-8766
▶CIRCLE 657

TIME-DELAY RELAY OPERATES IN 21 MODES

Simplify the selection of plug-in time-delay relays with the TRDU Series devices that include 21 operating modes. Any one of the 10 single-function or 11 dual-function modes is selected by transferring one or more of the six programming switches. Timing modes include delay-on-make, delay-on-break, interval, single-shot, recycling, motion detector, accumulating modes, inverted modes, and combinations of these. The multimode relays have industry-standard 8- and 11-pin base wiring. Time delay ranges from 0.1 sec. to over 1,705 hours. The TRDU Series operates at 12 or 24 V dc, and 24, 120, or 230 V ac. Its DPDT or SPDT isolated relay contacts are rated 10 A resistive at 240 V ac. Most parts in the TRDU Series are available from stock.

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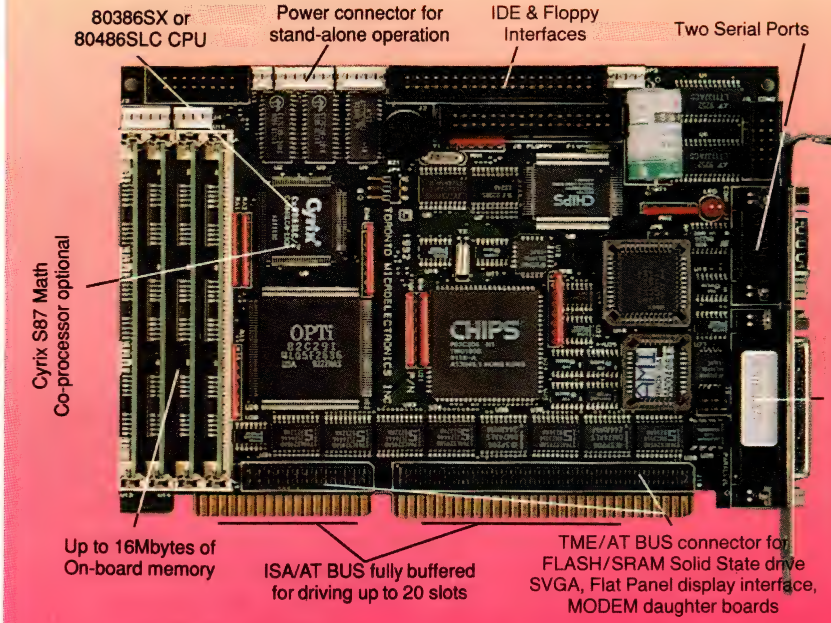

TME's F486SLC		COMPETITOR
✓	80386SX	Yes
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✓	16/25/33/40Mhz	?
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✓	Two serial ports with 10KV ESD Protection	No
✓	One Parallel Port	Yes
✓	Floppy & IDE interface	?
✓	Under 6.5W capability	?
✓	Watch Dog Timer	?
✓	Power Fail Detection	No
✓	Small form factor 4.75" x 7"	?
✓	Optional FLASH/SRAM Solid state drive, Flat panel display, VGA & SVGA interfaces	?
✓	Fully buffered AT BUS for driving up to 20 slots	No

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Tel: (905) 564-4833 • Fax: (905) 564-4768

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▼ PUSHBUTTONS ARE HEAVILY INSULATED

The 1200 Series line of pushbutton switches have a high insulation resistance of 1000 MΩ minimum at 500 V dc. These insulation values result from a heavy-walled polyamide case with high and thick molded barrier walls surrounding the switch terminals. Power ratings on the 1200 Series pushbuttons are 8 A at 125 V ac, 4 A at 250 V ac, or 4 A at 24 V dc. All switches features a 0.315-in.-diameter actuator that's available in black, green, red, or white for coding or equipment-enhancement applications. Both normally-open and normally-closed single-pole models are available. Butt-action, double-break silver contacts are rated for a minimum electrical life of 10,000 cycles at full load in an operating environment of –20° to 55°C. A typical model (the normally-open 1213A2) sells for $2.06 each in quantities of 1000 or more.

MORS/ASC
134 Water St.
P.O. Box 544
Wakefield, MA 01880-4444
(617) 246-1007
▶ **CIRCLE 659**

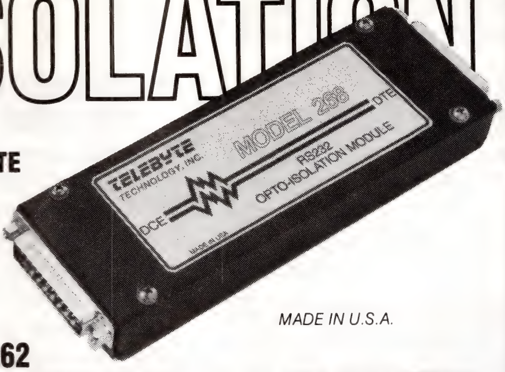
▼ ROTARY SWITCH SHIPS WITHIN 24 HOURS

The CK Series of single-deck rotary switches are competitively priced and will ship within 24 hours of order. Each part features an adjustable stop with a maximum of 12 positions. The series accommodates up to four poles per switch, with shorting or non-shorting contacts. A positive-index mechanism produces crisp, defined switching action. Options include bushings and shafts in various sizes to meet specific design requirements. Current-carrying capacity is 5 A with a contact rating of 150 mA or 250 V. Silver-plated brass contacts ensure a long service life in excess of 10,000 cycles. The CK Series is built from molded construction using glass-filled nylon. Delivery on standard commodity items is from stock. Customization is available upon specific customer request.

OakGrigsby Inc.
88 N. Dugan Rd.
Sugar Grove, IL 60554-0890
(708) 556-4200
▶ **CIRCLE 660**

ISOLATION

ELIMINATE
NOISE
AND
GROUND
LOOPS



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OPTO ISOLATED RS-232 TO RS-422 CONVERTER
Total isolation and conversion is provided with Model 262. Eliminates ground loops and withstands 10KV surges. Full duplex transmission up to 19,200 bps over 2 miles. **$142**

Model 268 • RS-232 OPTO ISOLATOR
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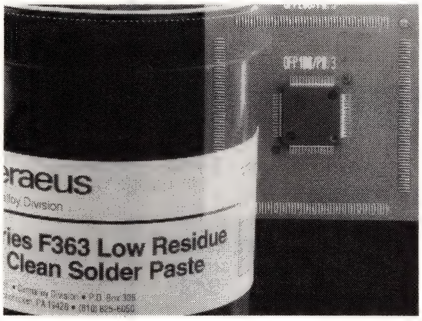
▼ NO-CLEAN PASTE DOESN'T MIND OXYGEN

A low-residue, no-clean solder paste is designed for reflow in a nitrogen atmosphere with high oxygen concentrations. The F363 solder paste can tolerate up to 5000 ppm of oxygen during processing, and leaves a clear residue of only 2.2 to 2.3% on the board. Processing of fine-pitch components to 12 mils is possible with excellent wetting, even on bare copper. There's no tendency for the paste to create solder beading on chip resistors and capacitors, and the very low flux residue is non-corrosive. Call for pricing and delivery.



Heraeus Inc.
Cermalloy Div.
P.O. Box 306
W. Conshohocken, PA
19428-0306
(610) 825-6050
▶**CIRCLE 661**

▼ DIE-ATTACH ADHESIVE REDUCES POPCORNING

A low-stress cyanate ester adhesive features a low modulus of elasticity to reduce warpage of large chips bonded to thin lead frames. The low warpage, in turn, helps make chips resistant to "popcorn" cracking, which can damage or weaken a plastic package and eventually cause the encapsulated chip to fail. The JM2500 adhesive exhibits moisture absorption similar to that of epoxies. However, cyanate ester ingredients can chemically react with moisture to form a thermally stable by-product. This dramatically reduces the explosive forces typically created by moisture flashing off during reflow, which causes popcorn cracking. Call for samples and pricing information.

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San Diego, CA 92131
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▶**CIRCLE 662**

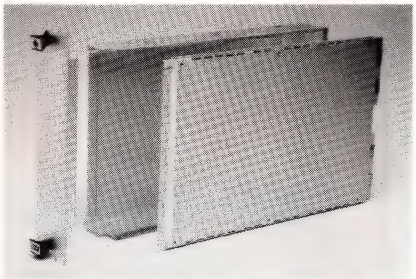
▼ CONDUCTOR SYSTEM USES INORGANIC BINDING

A unique inorganic binder used in the C1000 Conductor System delivers high conductivity and solderability for hybrid-circuit and component manufacturing. The C1000 System comprises four silver or palladium/silver pastes that provide excellent long-term aged adhesion and exceptional adhesion after thermal cycling. C1000 is the pure silver conductor, while C1003 is a 3:1 palladium/silver conductor, C1006 is a 6:1 palladium/silver conductor, and C1012 is a 12:1 silver/palladium conductor. All conductor pastes are cadmium-free and are compatible with the Heraeus air-fireable resistor systems. Call for pricing and additional information.

Heraeus Inc.
Cermalloy Div.
P.O. Box 306
W. Conshohocken, PA
19428-9306
(610) 825-6050
▶**CIRCLE 663**

▼ VXI HARDWARE KIT FITS WIDE MODULES

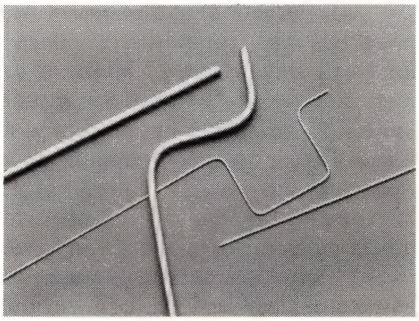
The Model 114343 VXIbus Hardware Kit is designed to package dual-wide VXI modules by overcoming the 0.8-in. component-height limitation imposed by single-width modules. It helps package modules with high components or modules with daughter boards. The clamshell-type design has metal side shields that close against the primary pc board. RF gaskets on the covers press against a ground strip on the board to provide an RFI-proof joint. An extruded front panel mounts directly to the board, and stays in place even when the side shields are removed. Numerous air slots are provided along the top and bottom edges of the covers to maximize the amount of cooling air blown over the module's components. The Model 114343 Hardware Kit includes a machined blank front panel, all necessary hardware, ejectors, and pc-board layout information. It's available now for $325. Delivery is in one to four weeks.



ICS Electronics Corp.
473 Los Coches St.
Milpitas, CA 95035-5545
(408) 263-5500
▶**CIRCLE 664**

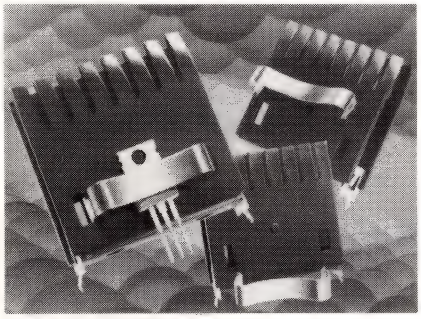
▼ LOW-LOSS CABLES HAVE HIGH STABILITY

A family of low-loss, semi-rigid coaxial cables exhibits high phase stability with temperature. The cable uses a special PTFE dielectric that typically has attenuation per 100 ft. that's 15-20% less than that of cables using standard dielectric. The special dielectric also has a lower coefficient of thermal expansion that does standard dielectric, which improves phase stability with temperature. Operating-temperature range is –100° to 250°C. The new low-loss cables are available with outside diameters of 0.047, 0.070, 0.0865, 0.120, and 0.141 in., and with a variety of male and female connectors. Cables can be purchased in sets matched for phase or amplitude. Call for pricing and availability.



Micro-Coax
a div. of UTI Corp.
Box 993
245 W. 5th Ave.
Collegeville, PA 19426-0993
(610) 489-3700
▶**CIRCLE 665**

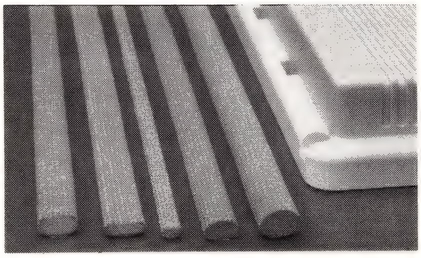
▼ HEAT SINKS WITHSTAND WAVE SOLDERING



Series 5308 high-rise heat sinks feature special tabs that lock securely onto pc boards during wave soldering. The heat sinks will accept one or two TO-218 or TO-220 semiconductor packages. Shur-Lock spring-action tabs, which go all the way through the pc board, prevent the heat sink from leaning or tipping during the soldering process. The slim design of the Series 5308 heat sinks increases surface area to improve cooling, while its twisted fins improve air flow. The tabs also serve as a 0.1-in. standoff for easy cleaning, and to permit routing of traces under the heat sink. The company's optional Kool-Klips stainless-steel spring clips snap into the heat sink to quickly attach plastic power devices. These devices can be mounted on one or both sides of the heat sink. Tests show that thermal efficiency increases 33% when using two devices. Call for pricing and delivery.

Aavid Engineering Inc.
One Kool Path
P.O. Box 400
Laconia, NH 03247-0400
(603) 528-3400
▶CIRCLE 666

▼ EMI GASKETS EXPLOIT LOW CLOSURE FORCE



Soft-Shield II self-terminating, low-closure-force EMI gaskets optimize the shielding of commercial electronics cabinets and metallized plastic housings. The gaskets provide up to 60 dB attenuation from 30 MHz to 1 GHz. The conductive yarn that's knitted as the gaskets' outer layer is self-terminating, requiring no secondary treatments. This also eliminates any metal-particle debris that's common with conventional wire-mesh gaskets. Its foam core needs a closure force of less than 1 lb/in., allowing for designs with fewer fasteners and thinner panels and more flexibility in enclosure design. The gaskets are easy to apply and can be supplied with a pressure-sensitive adhesive strip for quick and efficient mounting to cabinets and housings. Typical pricing for Soft-Shield II gaskets is under $1 per ft.

Chomerics Inc.
77 Dragon Ct.
Woburn, MA 01888-4014
(617) 935-4850
▶CIRCLE 667

DESIGN-IN WASHABILITY

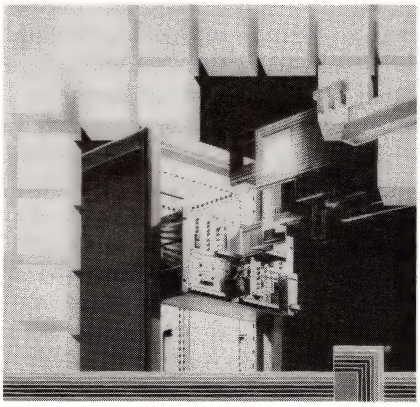
FREE Design Guide

When it comes to washable switches, NKK backs you with more sizes, more circuits and more quality than anyone else in the industry. NKK is your source for the first washable super-subminiature family, the smallest washable toggle, rocker and pushbutton devices, plus the world's most reliable switch contact mechanism (STC). So don't start your design without a free copy of our 456-page Design Guide and free tech support. Call 602/991-0942, FAX 602/998-1435 or write NKK Switches, 7850 E. Gelding Dr., Scottsdale, AZ 85260.

NKK® switches

▼ 19-IN. ENCLOSURES FILL 140-PAGE BOOK

A completely revised, full-color 140-page catalog details a broad line of electronic cabinetry. Featured is the Rittal iS (integrated system) of 19-in. installation systems. These include the Uniset/Varioset iS, a flexible card-frame system; the Vario Module iS, an aesthetically attractive instrument case with integrated card frame and 19-in. rack-mounting capabilities; and the updated Vario-Rack iS, which combines stability with functionality. An extensive range of system accessories for user-specific configurations complements the product information.



__Rittal Corp.__
3100 Upper Valley Pike
Springfield, OH 45504
(800) 477-4000
▶ **CIRCLE 668**

▼ PC-BASED SOFTWARE GIVES CROSS REFERENCE

NTE's full line of semiconductors, relays, and recently introduced flyback transformers are all cross-referenced in version 3.1 of the company's QuickCross software for PCs. The new version features an updated semiconductor cross-reference of 250,000 items and an updated relay section with 30,000 items. In addition to the flyback transformers, a selector guide on snap-in-mount capacitors has appeared. Version 3.1 has network support for up to 500 users and contains a time toggle to prompt users to request a new version in 13 months. Three disk sizes range in price from $6.75 per set.

__NTE Electronics Inc.__
44 Farrand St.
Bloomfield, NJ 07003
(800) 683-6837
▶ **CIRCLE 669**

▼ OEM SUPPLY CATALOG COVERS 125+ MODELS

More than 125 models of OEM power supplies, including many with 3-V main outputs, are covered in a catalog from Todd Products. The catalog includes data on fault-tolerant systems, self-cooling designs, and high-wattage supplies. It's profusely illustrated with full-color photos and detailed dimensional diagrams. Complete specifications are included for all models. A handy power-supply locator helps nail down the correct supply for your application.

__Todd Products Corp.__
50 Emjay Blvd.
Brentwood, NY 11717
(516) 231-3366
▶ **CIRCLE 670**

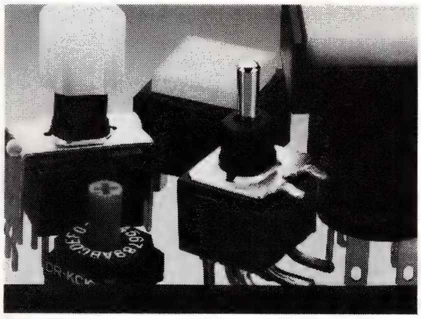
▼ QUARTZ COMPONENTS OFFER DIVERSITY

A diverse line of quartz components, ranging from microprocessor crystals and custom types to watch crystals, crystal oscillators, and monolithic crystal filters, is detailed in a 24-page catalog. Dimensional diagrams are complemented by complete specifications for each product. A form is included with which to request quotes on specific custom products.

__Cardinal Components__
22 S. Park St.
Montclair, NJ 07042
(201) 746-0333
▶ **CIRCLE 671**

▼ SWITCH DESIGN GUIDE IS NEWLY UPDATED

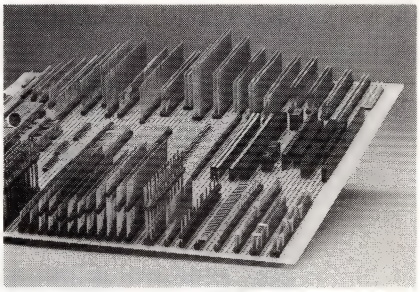
New listings for surface-mount, lighted, washable, and many other switch device categories have been added to the 1994/95 edition of NKK's engineering design guide. The guide provides information on how to specify and order any one of over a million different part numbers. Each of the reference's 54 sections contains Switch-Builder information that allows engineers to quickly and accurately identify the exact circuit, termination, actuator, rating, and hardware needed to complete a particular design. Several thousand precision dimensional drawings are included for simple cut-and-paste design-ins.



__NKK Switches__
7850 E. Gelding Dr.
Scottsdale, AZ 85260
(602) 991-0942
▶ **CIRCLE 672**

▼ EXPANDED CATALOG COVERS HEADERS, SOCKETS

A 60-page, newly revised catalog of pc-board connectors is far more comprehensive than the 40-page volume it replaces. Increased coverage is provided of 2-mm-centerline offerings, 0.050-in.-centerline products, and shunt interconnects in both 0.100- and 2-mm centers. An easy-to-use format presents technical data organized by centerlines. Pick-and-place packaging is available for both headers and sockets.

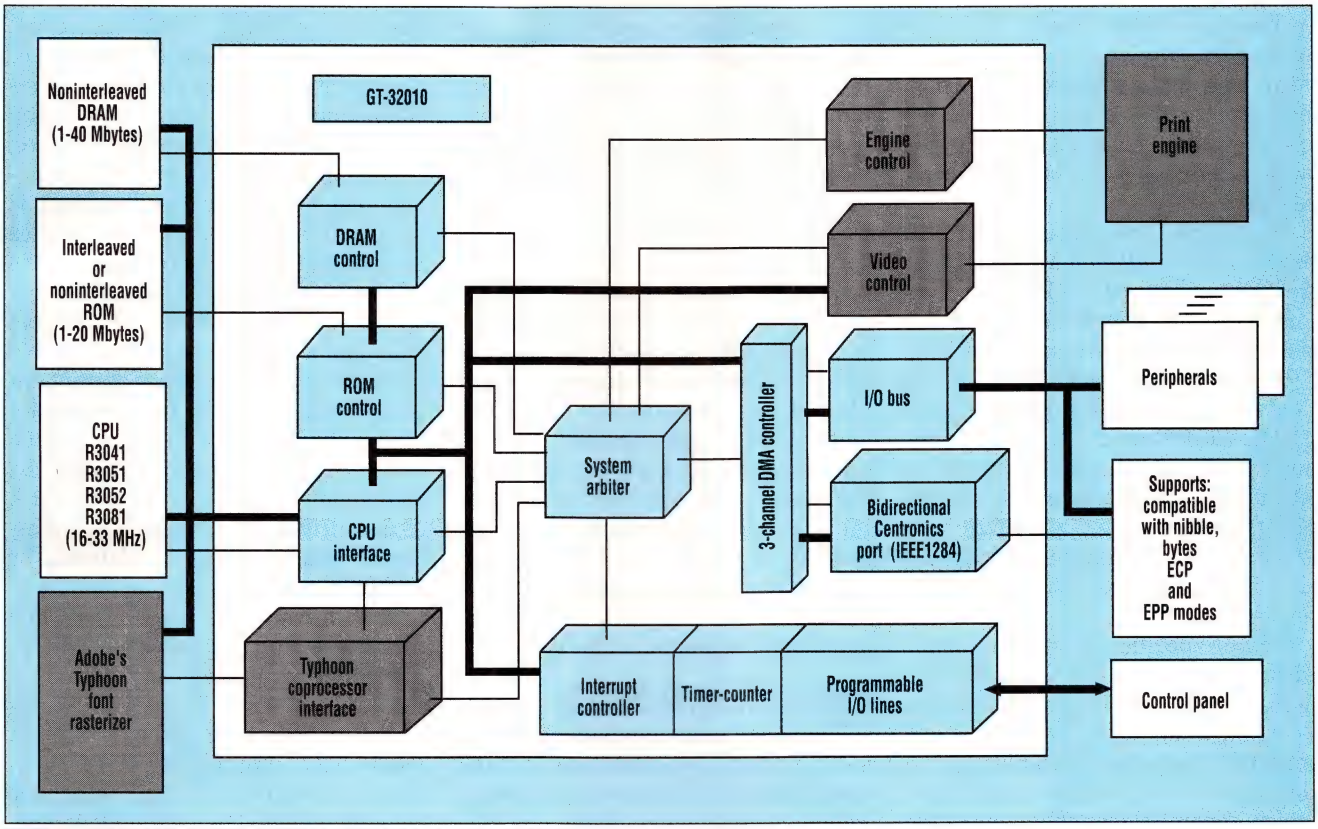


__Comm Con Connectors Inc.__
1848 Evergreen St.
Duarte, CA 91010
(818) 301-4200
▶ **CIRCLE 673**

▼ SELECTOR SPANS POWER SEMICONDUCTORS

An easy-to-use product-selector guide covers Powerex's entire line of power semiconductors. That spans transistor modules, rectifier and thyristor modules, and discrete high- and low-power products. The guide includes tables with basic parametric data, numbering systems for each product family, and package outlines.

__Powerex Inc.__
200 Hillis St.
Youngwood, PA 15697
(800) 451-1415
▶ **CIRCLE 674**


GT-32010
Noninterleaved DRAM (1-40 Mbytes)
Interleaved or noninterleaved ROM (1-20 Mbytes)
CPU R3041 R3051 R3052 R3081 (16-33 MHz)
Adobe's Typhoon font rasterizer
DRAM control
ROM control
CPU interface
Typhoon coprocessor interface
System arbiter
Engine control
Video control
3-channel DMA controller
I/O bus
Bidirectional Centronics port (IEEE1284)
Interrupt controller
Timer-counter
Programmable I/O lines
Print engine
Peripherals
Supports: compatible with nibble, bytes ECP and EPP modes
Control panel

1. EXCEPT FOR THE DRAM AND ROM, the GT-32010 controller developed by Galileo Technology provides all basic control and interface support for a laser-printer's RISC CPU. Direct printer support includes both print-engine and video-interface control, as well sa support for the Adobe Typhoon Font rasterizer coprocessor. In addition, the chip's counter-timer, DMA control channels, bus arbiter, bidirectional Centronics port, and 8/16-bit I/O bus add popular support functions to any control system. An alternative to the GT-32010, the GT-32011, eliminates the printer-specific features (video interface, engine control, Typhoon interface) and thus offers a lower-cost option.

INTEGRATED CONTROLLER SUITS LASER PRINTERS

DAVE BURSKY

Manufacturers of cost- or space-sensitive systems, such as laser printers and other peripherals, are constantly struggling to stay competitive. They must forever shrink the product's cost and size, while at the same time have it deliver even greater performance. To that end, many system developers have turned to RISC processors, such as the R3000, to serve as the embedded controller.

However, although RISC processors deliver impressive throughputs, they have not been known to deliver highly integrated solutions. Their "claim to fame" has been a small chip area for high-performance computing. Thus, highly-integrated *support* circuits for the RISC CPUs are essential to completing the system design.

To fill this support void, Galileo Technology created the GT-32010 system controller. Targeted at laser/page printers and other control systems, it works in conjunction with any member of the Integrated Device Technology R3051 family of MIPS processors. Together, the two chips form a complete subsystem (plus memory) that can control laser printers or other complex peripherals (scanners or other electromechanical devices).

The highly integrated controller circuit includes DRAM and ROM control to support the local RISC processor, three DMA channels for independent data movement without CPU intervention, and a bidirectional Centronics-compatible parallel port (IEEE-1284 Rev. 2) for communication to the host system. It also has an interrupt controller, a programmable 24-bit counter-timer, a configurable I/O bus, and a half-dozen programmable I/O lines for front-panel or other control functions.

Printer-specific resources start with a coprocessor interface to Adobe's Typhoon Font rasterizer, and a custom acceleration engine that can optionally be added. In addition, the chip contains both video- and print-engine control blocks that coordinate all the data transfers and motor control for the print engine.

Although the GT-32010's primary application is the page printer, its on-chip features suit it well for a wide variety of applications. A derivative product aimed at a wider variety of applications, the GT-32011, offers all the features except for the printer-specific resources, and is thus less expensive than the 32010.

Moreover, both chips can operate over a broad frequency range from 16 to 33 MHz, allowing system designers to create several performance/price points in a product family. Housed in an inexpensive 160-lead plastic quad-sided flat package, both system controllers will also be priced low enough that designers shouldn't feel they have to use every feature to make sure they get their money's worth.

Specific features that support page printers include the engine control block, which provides control and status lines to the print engine, and also provides the horizontal and vertical margin counters. The companion video controller block includes a four-entry (32-bit-wide) FIFO buffer and data serializer, and DMA support (with chaining) to move data into the FIFO. There's also a phase-locked loop to synchronize video data to the Linesynch signal and move data at up to 10 Mbits/s, and support for full-duplex printing. The PLL can be bypassed for engines that supply a video-clock signal at up to 33 Mbits/s.

In addition, the glue-less interface to Adobe's font-rasterizer coprocessor makes it simple to upgrade the printer by just dropping in the Typhoon chip—a big benefit especially to the Asian end-user markets that need the acceleration due to the complex character sets. The GT-32010 controls all of the data and address buffers that isolate the Typhoon from the address bus. As a master, it allows the Typhoon controller to access DRAM, ROM, and the I/O bus (for font cartridges). As a slave interface, the controller supports CPU reads and writes to and from the Typhoon.

LARGE MEMORY SPACE

The use of large numbers of fonts in laser printers also necessitates that the control logic be able to access a large address space. As a result, the GT-32010's designers included on the chip a DRAM controller that can address up to 40 Mbytes of non-interleaved DRAM, as well as a ROM controller that can access up to 20 Mbytes of interleaved or noninterleaved fixed memory. Both the DRAM and ROM banks support single-transfer reads and writes and burst reads, which allows the fast transfer of large blocks of data.

The bidirectional Centronics port included on the control chip supports both DMA- and CPU-controlled transfers, including nibble and byte transfers, and is compatible with the ECP and EPP enhancements to the Centronics port. Thus, not only can the host send data to the printer, but also the printer can send back a lot more in the way of status information—everything from status information on the paper or the toner to the size of the paper being used—depending on the sensors embedded and the control software used.

In addition to the parallel port, the configurable I/O bus included on the controller allows the chip to provide either an 8- or 16-bit 80186-style interface to control a wide range of I/O peripherals. The bus can look like two 8-bit channels and provide either DMA or non-DMA accesses, with CPU requests superseding DMA operations. It can perform 8-to-32-bit packing or 32-to-8-bit unpacking for DMA operations, and provide round-robin arbitration with the Centronics interface.

Also able to provide two 16-bit channels, the I/O bus can operate in 16-32 and 32-16 packing and unpacking modes to ease the CPU/Typhoon access to the I/O devices. The CPU can access any byte or half word. Bus switches support both big- and little-endian word structures. To support a variety of print engines and I/O devices, the I/O bus also allows the timing of its signals to be programmed. The I/O bus can also be used to attach additional storage, such as disk drives, or specialized I/O interfaces, such as network adapters, or PCMCIA peripherals.

An internal interrupt controller allows the chip to deal with 22 internal interrupt sources and six external sources. Each line permits individual bit masking and can thus be used with polling or interrupt-driven designs. Internal interrupt sources include the video DMA, line, band, page, timer-counter, I/O channel (3), Centronics (reset, read, write, equal), UART, parallel I/O, and some reserved lines. External interrupt sources come in through the six programmable I/O lines and are set as active-Low inputs.

Timing-related operations are controlled by a 24-bit programmable timer that will interrupt on the terminal count, and provide automatic reload from the valve register and continue count. In the counter mode, the unit will interrupt on a terminal count and stop counting; to restart the count, a new value must be written to the counter and the enable-bit set. ☐

PRICE AND AVAILABILITY

Housed in a 160-lead PQFP, the GT-32011 system controller sells for $17.95 apiece in lots of 10,000 units. Pricing for the GT-32010 will be determined shortly. Samples of both chips are immediately available, as is a reference design kit.

Galileo Technology Inc., 1735 N. First St., Suite 308, San Jose, CA 95112; Manuel Alba, (408) 451-1400. **CIRCLE 511**

HOW VALUABLE?	CIRCLE
HIGHLY	530
MODERATELY	531
SLIGHTLY	532

PRODUCTS NEWSLETTER

Serial EEPROMs Upgrade Interface

To compliment its family of Inter-IC and Microwire-compatible serial-interface EEPROMs, SGS-Thomson Microelectronics, Lincoln, Mass., has released a family of similar EEPROMs that are compatible with the 1-MHz serial-peripheral interface available on Motorola microcontrollers. The chips include the ST95P02C, 04C, and 08C, which are organized as 256 words by 8 bits, 512 by 8, and 1024 by 8, respectively. The memory chips include hardware and software write-protection schemes that start with a Write-Protect pin to lock out writes when the signal on the pin is low, and include several nonvolatile status bits that allow blocks of memory to be selectively write-protected under software control. The memories are organized as 16, 32, or 64 pages of 16 bytes, and up to 16 bytes in any page can be written in one nonvolatile write cycle. Programming is self-timed; maximum cycle time is 5 ms. The chips have a guaranteed endurance of 1 million erase/write cycles, with minimum data retention of 10 years. They come in 8-pin miniDIPs or SO packages, and can operate from one 3- to 5.5-V supply. Available now, samples are $1.45 each in lots of 1000. Call Pierre Matte, (617) 259-2527. *DB* **CIRCLE 601**

Development Kit Eases Serial EEPROM Designs

A serial EEPROM designers kit assists engineers in programming and creating applications based on serial EEPROMs. The collection of serial EEPROMs, PC-hosted software, and programming card assembled in the kit by Microchip Technology, Chandler, Ariz., offers tools to speed system designs and ensure proper component selection. The software tools provided in the kit allow designers to factor in the application environment in the selection and evaluation process in the calculation of the erase/write endurance, ensuring a more robust and reliable system design. Included is SEEVAL, a serial EEPROM programming and evaluation system, the total Endurance software disk, which contains the application analysis and design tools and a tutorial and hypertext help file, a serial EEPROM data handbook, and various support materials. Initial price is $93.24; $149 after Sept. 30. Call Peter Sorrells, (602) 786-7200. *DB* **CIRCLE 602**

Smart Battery Charger Trims Charging Time

A microprocessor-based battery charging controller, the ATC106 provides a fast-charge solution for either NiCd or NiMH batteries. Incorporating the latest charging techniques on its on-chip memory, the circuit, from Shoreline Electronics, Santa Clara, Calif., can help to charge batteries in as little as 15 min. As part of the on-chip circuitry, the ATC106 includes a "Zero Delta V" circuit optimized specifically for NiMH batteries, which allows the number of cells and charge current to be easily adjusted. It also includes a 15-hr. trickle-charge termination to stop overcharging damage to NiMH batteries. A self-test feature is included to test all critical functions of the completed charger, assuring the system is functioning properly. Features that can be tested include maximum timer, full-charge indication, $\Delta T/\Delta t$ sensitivity, $-\Delta V$ sensitivity, fast-charge mode, discharge mode, and LED test. In 1000's, the ATC106 is $3.50 each in a 24-lead shrink DIP or 24-lead plastic SOP. Call Sun Choi, (408) 987-7733. *DB* **CIRCLE 603**

PCB Tools Introduce PC-Network Licensing

Accel Technologies, San Diego, Calif., has a new program of floating-network software licensing for its PC-based TangoPRO for Windows line of pc-board design tools. With Tango Network Licensing, users can check out a license of TangoPRO from a bank of licenses resident on the network. The system saves disk space, reduces the licenses required to service a workgroup, and eliminates the need for software-security devices on each computer. Network-based floating licenses, which are popular on Unix-based workstations, weren't promoted in PC-based design automation because PCs don't contain unique address IDs. Working with software security maker Rainbow Technologies, Irvine, Calif., Accel implemented a network-security scheme for its Windows-based EDA tools, which provides the same benefits as a Unix-based system. The price for the network floating license is set as a surcharge over the single-license price. At quantity one, the network license surcharge is 50%, with no quantity discount. For three, the surcharge is 25%. As quantities go up, the discount increases. Tango Network Licensing will be available in September. Call (800) 488-0680 or (619) 554-1000. *LM* **CIRCLE 604**

Edited by Clifford Meth

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1EDh4c

SWISS-ARMY MODEM CHIP HANDLES DATA, FAX, VOICE

The business traveler's fantasy of a compact electronic office has taken a large step towards reality with the development of a pair of "Swiss Army" chips, which can be used as a fax or data modem, an answering machine, and a telephone handset for wired or cellular applications. The CL-MD1414 family of multipurpose modems was designed to provide a complete set of bundled features for desktop, laptop, or even handset-based products.

The two-chip set is designed to operate using an external ROM, EPROM, or flash memory, allowing it to easily be configured to operate under nearly any international communications standard. Subroutines for use in the modem's firmware, which provide support for most international fax, data, and telecommunication standards, is supplied by Cirrus at no extra charge.

For data transmission, the modem is capable of supporting all standard protocols, up to V.32bis, yeilding data rates of up to 14.4 kbits/second. The device provides error correction using either TIA standard V.42 or Microcom-licensedMNP2-4 techniques. Data compression up to 4:1 may be achieved using the chip's V.42bis or MNP5 algorithms.

Used as a fax modem, the chip set supports all standard protocols for Class 1 and 2 transmissions, including the V.17, V.29, V.27ter, and V.21, permitting data rates up to 14.4 kbits/second. Standard and fine resolution modes are also software selectable.

In addition to complete modem and fax capability, the engineers at Cirrus found enough real estate on their chips to include a sophisticated telephone network interface and voice handling capability. Using the embedded voice mode "AT" command set, the modem may be commanded to function as a standard telephone handset. In this mode, the chip can originate or receive calls, with only the addition of an external speaker and microphone.

When receiving calls, the incoming message may be digitized at a variety or rates (4800 to 22050 samples/second) and passed to an external storage device for playback at a later time. To save memory space, either ADPCM, linear, or CL1 compression algorithms may be selected. The chip also supports a "caller ID" function to permit programmed or manual call screening. Using these features, designers can easily give a computer the capabilities of a sophisticated answering machine or multiuser voice mail system.

The CL-MD141U chip family uses a single +5V supply and has a simple, flexible interface structure, for easy application in a variety of products. In conventional computer applications, the CL-MD141-UN may be interfaced directly to any ISA bus as a selectable address COM port with no external decode logic. For PCMCIA applications, the CL-MD141-UNP connects directly to a PCMCIA 2.1 bus and has a programmable CIS (internal card information structure) memory.

Both chips provide an MNP 10 interface for cellular applications. Firmware and user-specific configuration data may be easily stored in an external ROM via the chip's built-in memory interface. The interface also supports RAM or flash memory, permitting firmware changes to be made as needed. A separate memory path may be interfaced to an NVRAM if desired.

The chip set come in VQFP packaging, making PCMCIA applications possible. The compact size and low power consumption (450 mW operating, 40 mW standby) make it a good candidate for portable applications, as well as desktop computers where motherboard space is at a premium.

Both chip sets will be available in sample quantities early in the fourth quarter of 1994, with full production anticipated soon after. Pricing will be $50 for either chip set in quantities of 1000.

Cirrus Logic Incorporated,
3100 West Warren Avenue,
Freemont, CA 94538; (510) 623-8300.

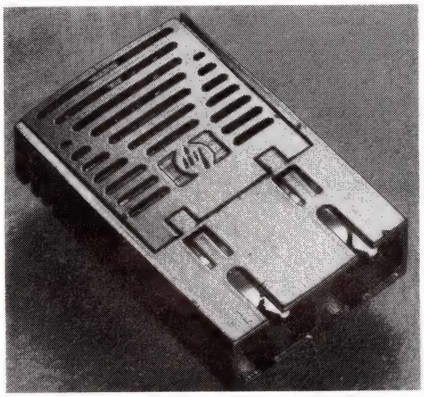
CIRCLE 700

■ *LEE GOLDBERG*

MODULAR FIBRE-CHANNEL TRANSCEIVERS

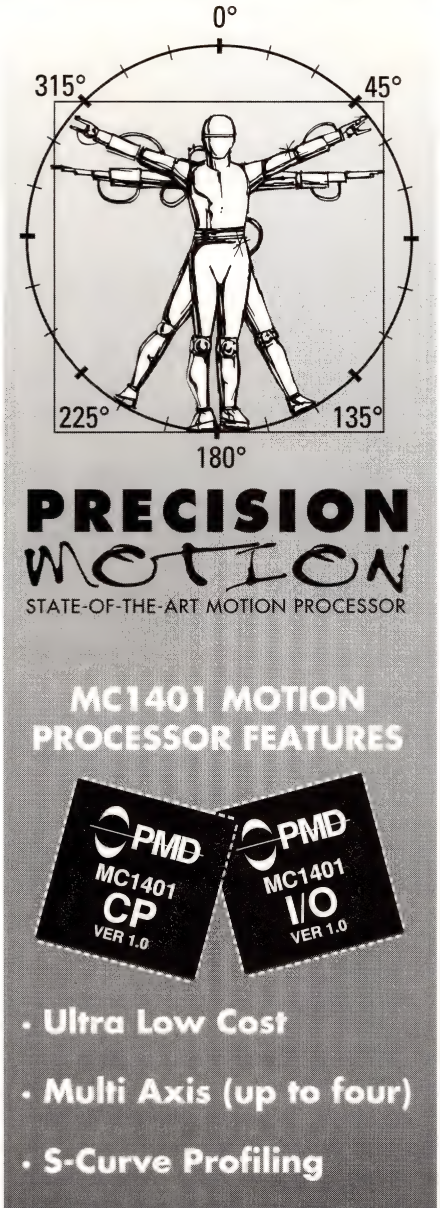
The HFBR-5301 and HFBR-5302 Fibre-Channel receivers provide system designers with low-cost fractional Gbit links in the new standard 1X9 SIP package. These compact modules use a 1300-nm LED to provide data rates of 133 and 266 Mbitsper second.

Both transceivers can interface to either 62.5/125-μm or 50/125-μm multimode fiber-optic cables via their integral duplex SC optical-fiber connectors. The transceivers mount directly on a circuit board via the nine-signal pins and two solder posts, which provide sturdy mechanical support.



In quantities of 1000, the 133-Mbits/s HFBR-5301 is priced at $80, while the 266 Mbits/s HFBR5302 costs $100. Both units are available immediately. LG

Hewlett Packard Company, 5301 Stevens Creek Blvd., Santa Clara, CA 95052-8059; (800) 357-7715, ext. 8364. CIRCLE 701



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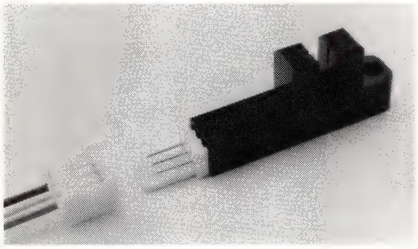
NEW PRODUCTS

COMPONENTS

INFRARED SENSOR INCLUDES CONNECTOR

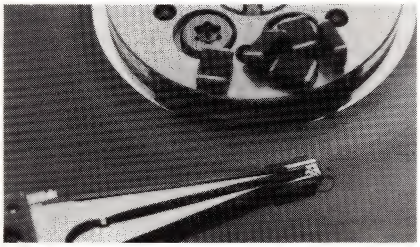
The HOA7000 Series connectorized infrared sensor is a transmissive assembly with a TTL output. The sensor features a built-in connector for easy assembly into equipment. It consists of an infrared emitter and a Schmitt trigger detector enclosed in a polycarbonate housing. Detector switching occurs whenever an opaque object passes through the slot between the emitter and detector. The integral, three-pin connector simplifies installation to standard mating connectors. With its narrow 6:8-mm width, the sensor's package is easily stacked for multichannel detection. Open-collector or totem-pole outputs are offered. Typical applications include data storage, duplication products, instrumentation, and vending machines. Price is about $2.80 in lots of 25,000. Delivery is from stock. DM



Micro Switch, a Honeywell Div., 11 W. Spring St., Freeport, IL 61032; (800) 367-6786. **CIRCLE 703**

MULTILAYER FERRITES KILL 1500 MA OF EMI

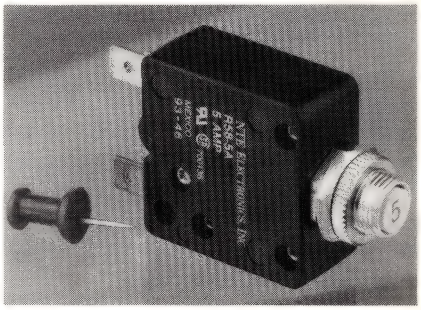
A surface-mounted EMI suppressor chip offers greater amperage than do standard chip beads. The BCB-1812-1.5A chip has a maximum rated current of 1500 mA. Typical amperage for such devices is about 300 mA. The device's higher rating suits it for applications in which EMI must be suppressed or attenuated while high current is maintained. These include motor-start/stop operations in disk or tape drives or any other application involving large current spikes. The chip comes in a standard 1812 package (4.5 by 3.2 by 1.5 mm). Impedance is rated at 125 Ω at 100 MHz. Operation is from –55 to 125°C. Pricing is $0.085 in lots of 100,000 with packaging in reels of 500. Delivery is in four to six weeks. DM



Associated Components Technology, 11575 Trask Ave., Garden Grove, CA 92643; Erik Dieckhoff, (714) 636-2645. **CIRCLE 705**

THERMAL BREAKER PROTECTS CIRCUITRY

Bushing mounting, 0.250-in. quick-connect terminals, a visual trip indicator, and a reset button that cannot be manually tripped are all featured in the R58 Series of thermal circuit breakers. The line consists of 12 different UL- and CSA-rated devices ranging in rating from 1 to 20 A. Operating at a maximum voltage of 50 V dc/250 V ac, the breakers offer dielectric strength of 1500 V ac rms and will continuously carry 100% of rated current. Call for pricing and delivery. DM



NTE Electronics Inc., 44 Farrand St., Bloomfield, NJ 07003; (800) 631-1250. **CIRCLE 706**

PLASMA DISPLAYS BOAST EASY READING

Excellent viewing characteristics define a line of full-field, dc-plasma displays. Using a 128-by-64-pixel format, two different viewing areas are offered: 5.10 by 2.55 in. (APD-128G064) and 12.75 by 6.35 in. (APD-128G064A and A-1). The displays combine neon-orange characters and graphics with high brightness and a 150° viewing angle. Prices in lots of 100 start at $120. DM

Dale Electronics Inc., 1122 23rd St., Columbus, NE 68601-3647; Dale Raysby, (402) 563-6413. **CIRCLE 707**

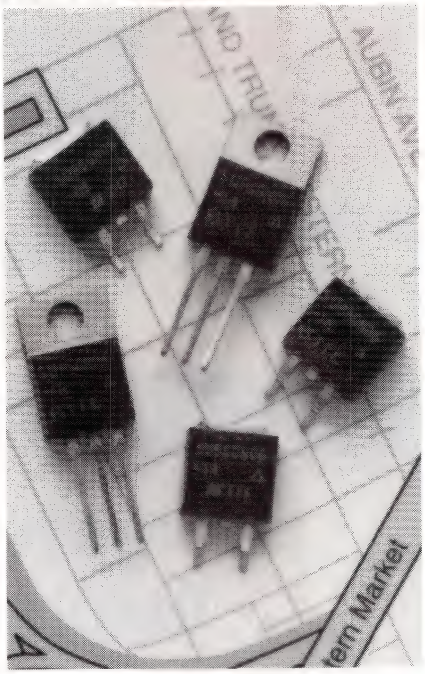
LOW $R_{DS(ON)}$, 60-V POWER MOSFETS STAND UP TO AUTOMOTIVE USES

With maximum on-resistance of just 8 mΩ, the TrenchFET line of power MOSFETs are claimed as the industry's first surface-mount MOSFETs with such a low $R_{DS(ON)}$ rating. The devices, which are based on a proprietary Siliconix technology, are initially available in TO-220 and TO-263 (D^2PAK) packages.

The five-product family features a 60-V breakdown voltage and 175°C maximum junction temperature to meet the harsh demands of the automotive environment. For applications such as motor and pump control, HVAC systems, fuel pumps, and braking systems, the devices provide maximum on-resistance ratings ranging from 8 to 18 mΩ.

Compared to typical n-channel products, the TrenchFET power MOSFETs offer on-resistance specs that are so low that the need for heat sinking is dramatically reduced, which lowers parts counts and assembly costs. The surface-mount TO-263 packages also simplify the design and lower the manufacturing costs of automotive assemblies such as power steering, window lifts, and seat-positioning motors.

All five of the MOSFETs are based on Siliconix's trench vertical power-MOSFET technology. Initially, the devices offer transistor-cell densities in excess of 8 million cells/in.^{2}.



The low on-resistance values reduce the need for paralleling MOSFETs and offer lower conduction and switching losses than typical 60-V parts.

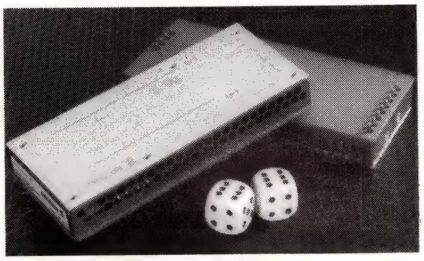
Samples and production quantities of all five TrenchFET power MOSFETs are available now. Pricing in large OEM lots ranges from $0.96 to $1.93.

Siliconix, 2201 Laurelwood Rd., P.O. Box 54951, Santa Clara, CA 95056-0951; (800) 554-5565, ext. 30. **CIRCLE 708**

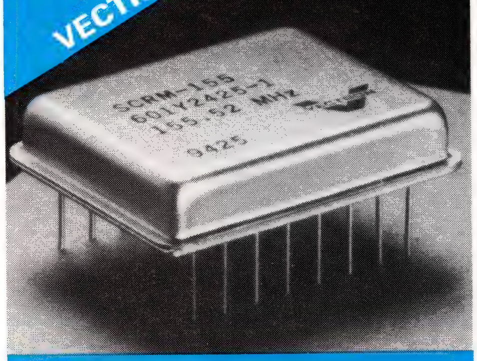
■ *DAVID MALINIAK*

DC-DC POWER MODULES DELIVER UP TO 150 W

The first two products in a family of high-density dc-dc converters are now available. Model PKU 4111 PI is a single-output, 5-V, 150-W unit; and model PKU 4110 PI is a 3.3-V type with 100-W output. Both offer input-voltage ranges of 36 to 72 V dc to cover 48/60-V systems. Features include a pinout that duplicates that of AT&T's FW Series with a smaller footprint and a maximum 100°C baseplate temperature. The units' enclosure offers through-ventilation cooling, yet permits water washing after soldering. Input-to-output isolation is 500 V dc. Parallel operation is permitted by means of a separate parallel-mode pin. Pricing is $155 each in lots of 100. DM



Ericsson Components Inc., 403 International Pkwy., Richardson, TX 75081; Richard Hoag, (214) 997-6561. **CIRCLE 709**



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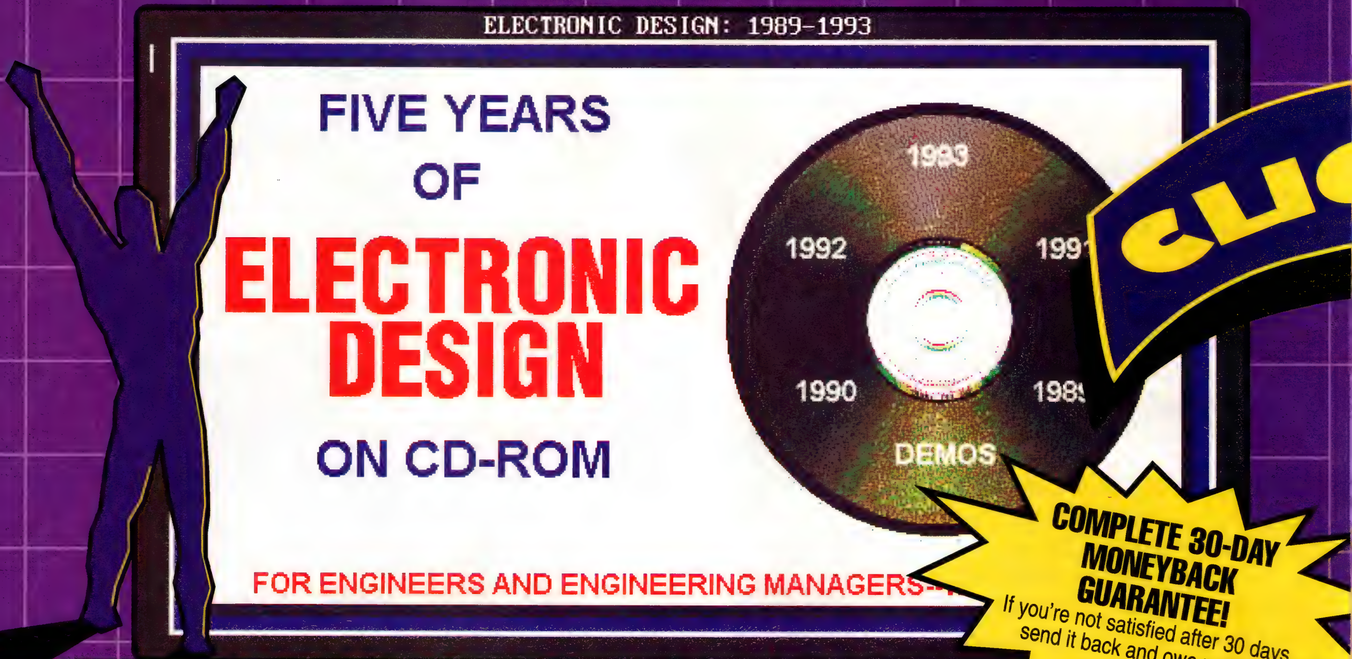
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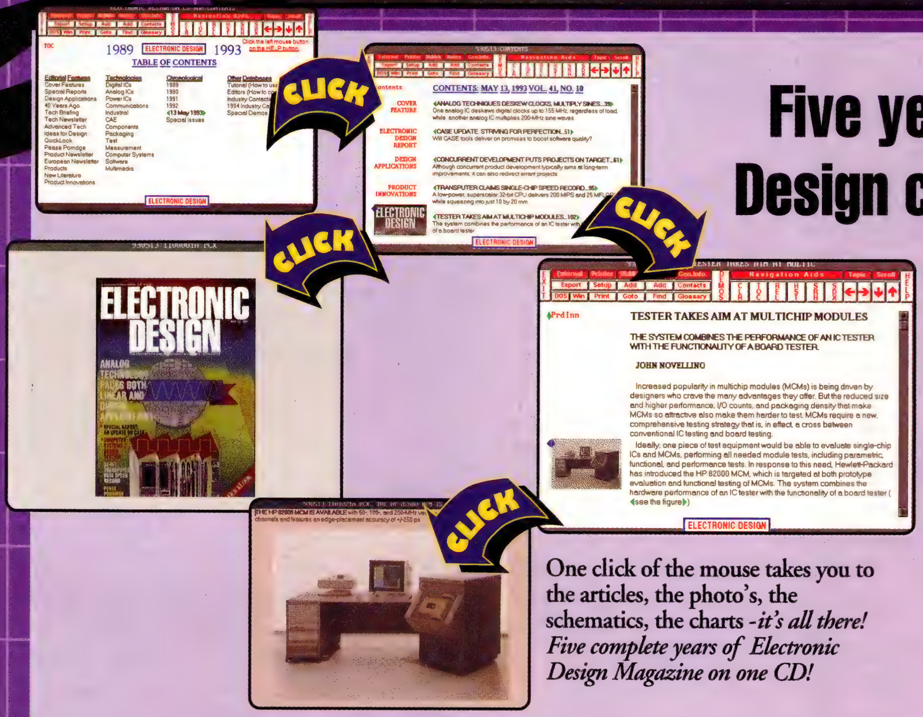

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TESTER TAKES AIM AT MULTICHIP MODULES

THE SYSTEM COMBINES THE PERFORMANCE OF AN IC TESTER WITH THE FUNCTIONALITY OF A BOARD TESTER.

JOHN NOVELLINO

Increased popularity in multichip modules (MCMs) is being driven by designers who crave the many advantages they offer. But the reduced size and higher performance, I/O counts, and packaging density that make MCMs so attractive also make them harder to test. MCMs require a new, comprehensive testing strategy that is, in effect, a cross between conventional IC testing and board testing.

Ideally, one piece of test equipment would be able to evaluate single-chip ICs and MCMs, performing all needed module tests, including parametric, functional, and performance tests. In response to this need, Hewlett-Packard has introduced the HP 82000 MCM, which is targeted at both prototype evaluation and functional testing of MCMs. The system combines the hardware performance of an IC tester with the functionality of a board tester (see the figure)

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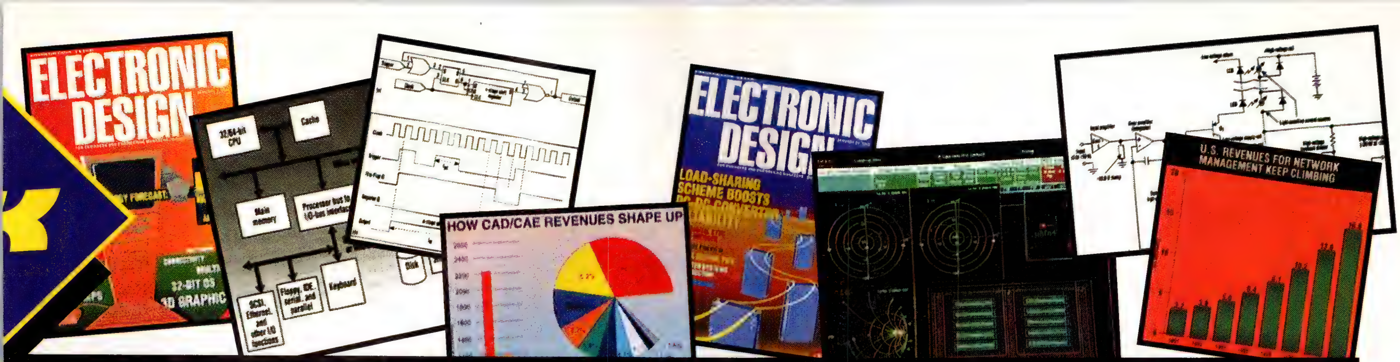
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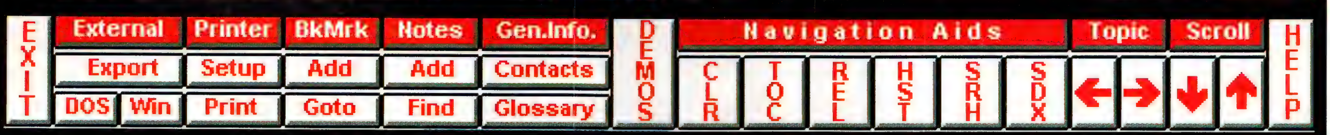

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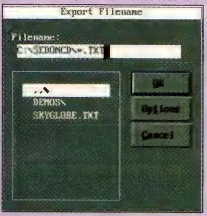

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The **Export** button will export any or all of an article based on your selection.

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DOS brings you to the DOS prompt screen and **Win** takes you into Windows™ without quitting the application. These buttons make it easy for you to return to Electronic Design Magazine, where you left off, without re-launching.

Printer Commands

Setup & Print - This feature allows you to print articles, editorials, glossaries, illustrations, and even photos *(if your printer is capable)* directly from this CD. Great source for reference.

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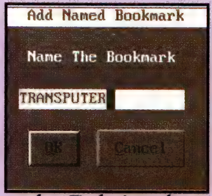
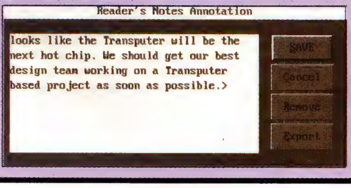
BkMrk - Bookmarks flag topics for future reference, just like using a bookmark in a real magazine. Mark a spot, and the bookmark is stored even if you quit.



Name The Bookmark TRANSPUTER

GOTO brings you back to your bookmarks. Deleting them is just as simple.

Notes - Add and find your own notations. Notes stay until you delete them, even after you quit.



looks like the Transputer will be the next hot chip. We should get our best design team working on a Transputer based project as soon as possible.>

Gen. Info - Complete reference

Contacts - Company names, addresses, contact names, phone numbers- all of the information you need to follow up.

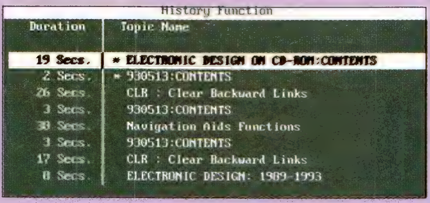
Glossary - Full article glossaries, provided by the Editors of Electronic Design magazine. The CD also comes with **WORD LINK**, which allows you to click on any word within the article and if it's in the glossary, the definition pops up. When you're done, a simple click and it's gone.

Navigation Aids - Magellan you're not, and you don't need to be!

All the aids you'll need to motor your way through this CD in no time flat.

CLR - *Clear Back Links* - Because every article you move to loads into RAM, this function allows you to clear articles you've finished. This frees up RAM for you to continue.

TOC - *Table of Contents* - Takes you directly to the Volume Table of Contents (the whole year) with special links provided to Issue T.O.C.



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 2 Secs.   * 930513:CONTENTS
26 Secs.     CLR : Clear Backward Links
 3 Secs.     930513:CONTENTS
38 Secs.     Navigation Aids Functions
 3 Secs.     930513:CONTENTS
17 Secs.     CLR : Clear Backward Links
 8 Secs.     ELECTRONIC DESIGN: 1989-1993
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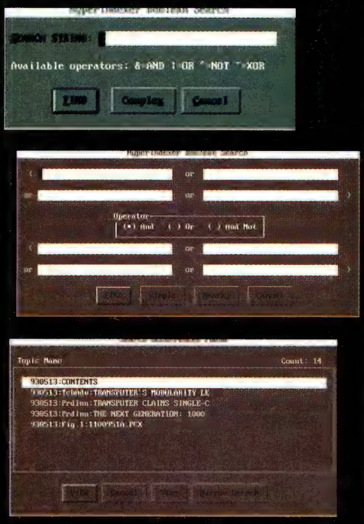
REL - *Show-Related Articles* - Calls up a list of, and lets you move to, related topics.

HST - *Show-Related History* - Shows each topic visited during your current session and how long you were there, and then lets you return to previous topics.

SEARCH dialog boxes

Simple search (top), Complex Search (center), and Search occurances found (bottom).



Available operators: &=AND |=OR ^=NOT ~=XOR

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930513:PrdInn:TRANSPUTER CLAIMS SINGLE-C
930513:PrdInn:THE NEXT GENERATION: 1000
930513:Fig 1:1100951A.PCX
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SRH - *Search* - Conduct simple, complex or proximity indexed searches.

SDX - *Subject Index* - A hierarchical list of key subject areas compiled by the Editors of Electronic Design. The index also allows direct access to related topics.

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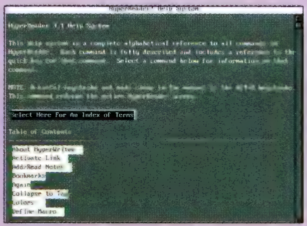


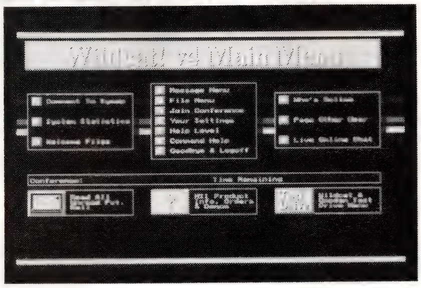
MINIMUM SYSTEM REQUIREMENTS

- ☞ 80386 PC or better
- ☞ VGA video card adaptor w/640 x 480 pixel resolution 16 colors.
- ☞ 1 meg ram
- ☞ MS-DOS Version 3.1 or later

BBS SOFTWARE ENHANCED FOR FLEXIBILITY

To meet demand for features that allow bulletin board systems (BBS) to be tailored individually, Mustang Software's developers rewrote Wildcat! BBS software from top to bottom. As a result, version 4 of the software has 250 enhancements, including a GIF thumbnailer, which enables callers to preview miniature versions of multiple picture files on screen before downloading a specific file.

Version 4 also incorporates an improved chat capability, which eases live, online conversations through the bulletin board system. The sysop now has more organizing power to set up and manage parties to specific conversations and to speed up exchanges.



With version 4, sysops can alter the four-menu structure—main, message, file, and sysop—to produce their own menu choices based on individual BBS requirements. Sold separately from the software, a new programming language, wcCODE, includes an integrated development environment with compiler, editor, and help screens.

Said to be easy to use, wcCODE is a QuickBasic language that enables the sysop to write BBS applications without having extensive programming experience or detailed knowledge of BBS elements like modems. Other enhancements include an improved organizing system that increases database search-and retrieval speeds tenfold compared with previous versions. Version 4 provides for 32,760 separate conference and file areas compared with 1000 in earlier versions.

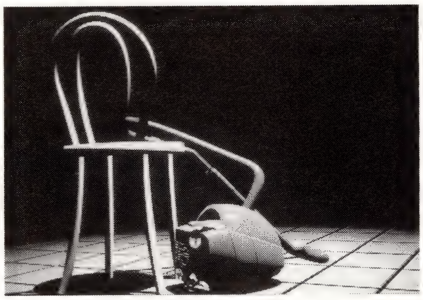
DOS-based, Wildcat! version 4 starts at $129 for a single-line package; a corporate version for 10 lines is $249; a 250-line version is $499. The wcPRO utilities, which includes a program for automatic faxing of documents, is $99; the wcCODE language is $149.

***Mustang Software Inc.**, Post Office Box 2264, Bakersfield, CA 93303; (805) 873-2500; fax -2599; bulletin-board service - 2400.* **CIRCLE 710**

■ *SHERRIE VAN TYLE*

DESIGN AND RENDERING SOFTWARE IS UPGRADED

Version 6 of Conceptual Design & Rendering Software has an improved user interface and new rendering features. CDRS version 6 gives several levels of control: During concept development, dynamic sculpting enables designers to work free-form by pushing, pulling, and twisting a surface to define a shape.



The model can be refined with boundary influence and surface tangent controls that allow for precise editing of surfaces and tangents as they relate to one another. Surface master/slave relationships control the surface relationships by determining the influence that one shape or surface can exert on another joining surface. Bump-mapping, a new feature, gives enhanced realism of rendered surfaces where textures is part of the object. Designers can toggle between vectors and shaded polygons to verify surfaces fast. Contact the company for prices. SVT

Evans & Sutherland, 580 Arapeen Dr., Salt Lake City, UT 84108; (801)582-5847;fax-9413. **CIRCLE 712**

FAX SOFTWARE ACCESSES DATABASES

With FaxBase III, users can access a database through a fax machine in real time. The system reads and writes information to the database, in response to input received from a push-button phone, and sends the information to the caller's fax machine. FaxBase III uses electronic data interchange (EDI) technology that uses real-time access to selected portions of the supplier's database. It permits a dynamically created file to be combined with a static document to produce custom reports and respond to specific requests. The software supports such databases as Paradox, dBase, Btrieve, ASCII, SQL, and operating systems such as DOS, Unix, and Novell Inc.'s Netware. It starts at $5995. SVT

Fax On Demand Inc., 15101 Surveyor Blvd., Addison, TX 75244; (800) 329-1777; fax (214) 386-4170. **CIRCLE 712**

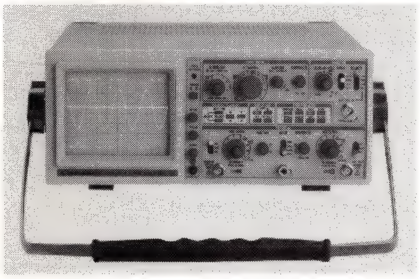
IMPROVE COLOR GRAPHICS ON A PC OR A MAC

High-impact color graphics can be created for presentations and reports using the ColorUP color software utility. The software works with either PC or Macintosh platforms. It consists of two components, the Palette Chooser and the Explorer. The Chooser offers a comprehensive library of ready-to-use media-aware color palettes. The Explorer is an interactive encyclopedia filled with color information and experiments designed to improve the user's understanding of color deployment. The 1500-color palette consists of combinations that have been tested for the primary forms of media output. Output can be sent to such applications as Harvard Graphics, Lotus Freelance, Microsoft PowerPoint, Aldus Persuasion and FreeHand, Micrografx Charisma, Adobe Illustrator, and Corel Draw. The entire setup consumes about 10 Mbytes of hard-disk space and requires Windows 3.1 and 4 Mbytes of RAM on the PC and System 6.0 and 2 Mbytes on the Mac. Both versions of ColorUP are priced at $99.95. RN

Pantone Inc., 590 Commerce Blvd., Carlstadt, NJ 07072; (201) 935-5500. **CIRCLE 713**

60-MHz, 20-MSAMPLE/S DSO HAS RS-232 PORT

The Model 2560 is a two-channel digital-storage oscilloscope with a 20-Msamples/s sampling rate and 60-MHz bandwidth. The scope makes cursor measurements of voltage, time interval, frequency, and pre-trigger. An RS-232 port allows users to send waveforms to a computer for processing, or print hard copies on an HP-GL plotter. Real-time sampling is automatically invoked for time-base settings of 10 μs/div. and slower. At 5 μs/div. and faster, sequential equivalent time sampling is used. In real-time mode, storage is 2 ksamples/channel. In equivalent sampling mode, storage is 1 ksample/channel. Triggers include automatic, normal, TV-V, and TV-H. X-Y operation is also provided. The Model 2560 costs $2395. JN



B+K Precision, 6470 W. Cortland St., Chicago, IL 60635; (312) 889-1448. **CIRCLE 714**

HANDHELD PROGRAMMER ALSO DOES EMULATION

The Orbit 32 handheld device programmer features fast emulator capability. Users can connect the instrument to the target system, reducing development times by eliminating the need to program devices until the code has been optimized. The 170-by-100-mm unit, which has a 32-pin wide-blade ZIF socket, can program EPROMs to 8 Mbits, EEPROMs, and flash devices. It can also program some CMOS PROMs and serial EEPROM devices in 0.3- and 0.6-in. pitch DIPs. All device libraries reside on-board in a nonvolatile memory, which can be upgraded through a PC or directly through the socket. The Orbit 32 costs $795 and is available from stock. JN

Stag Microsystems Inc., 1600 Wyatt Dr., Santa Clara, CA 95054; (408) 988-1118. **CIRCLE 715**

TOOL CREATES RANDOM-LOGIC BIST FOR ICS

As a random-logic built-in-self-test (BIST) tool, BIST1 addresses the problems posed by large ICs because it tests all parts of the circuit at once instead of serially. The software includes everything needed to modify a circuit to incorporate BIST. Incoming circuits are audited and analyzed and a set of flip-flops are chosen. Based on known allowances for overhead, users can specify a maximum number of flip-flops. Many vendor libraries are supported. BIST1 outputs the modified circuit in the same format with the circuit's hierarchy preserved. BIST1 runs under Unix 4.1 or higher on Sun-4 or Sparc Station workstations. The package will be available in beta version in the third quarter and in the full commercial version in the fourth quarter. JN

AT&T Design Automation, Room 2B-247, 1247 Cedar Crest Blvd., Allentown, PA 18103-6025; (800) 875-6590. **CIRCLE 716**

ASIC INCREASES BOUNDARY-SCAN ACCESS

The ParaScan ASIC is a test-access device that expands the test coverage of Texas Instruments' Asset Diagnostic System during multichip module and printed-circuit board interconnect testing. The ASIC increases access to the unit under test during embedded tests and performs non-1149.1 (boundary scan) logic testing. It also enhances test coverage by allowing testing through the edge connector. The ParaScan comes in a 144-pin quad flat pack. It has 66 bidirectional inputs and outputs, each having its own control cell. The BC-7 type bidirectional cell design allows the cell to capture its driven value from the pin. The ParaScan costs $225, including documentation and product support service. A 144-pin QFP socket costs $29. JN

Intellitech Corp., 66 Route 25, Meredith, NH 03253; (603) 279-6308. **CIRCLE 717**

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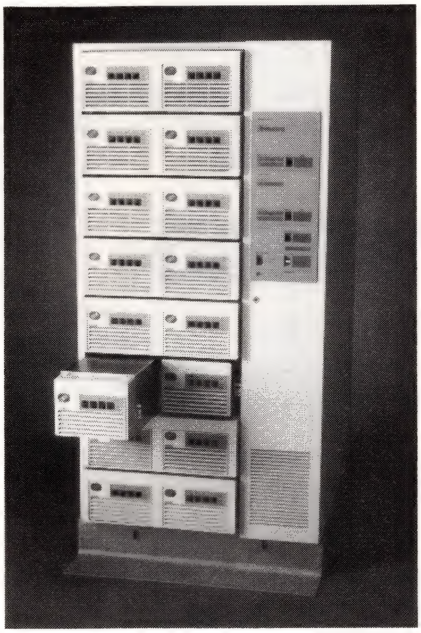
READER SERVICE 176

HIGH-END DISK ARRAY OFFERS RAID 5

A family of RAID 5 storage products boast high performance and fault tolerance. The RAMAC series currently consists of two members, the Array Subsystem and the Array DASD.

The Subsystem attaches directly to the host system and it is built with an integrated array controller to supply a host of format options to accommodate interoperability with both current and older DASD products.

The Array DASD connects to cached models of the 3990 Storage Control, supplying the 3990 volume format as well as all the features and functions of the 3990. Because almost no programming changes and few application programming changes are required, both storage units offer software transparency to the user.



Both units are designed with 3.5-in. 2-Gbyte disk drives in drawers, where each drawer contains four drives. The drawer cache also has a separate path to each drive, with each path able to transfer data to or from the cache concurrently. The RAMAC Array DASD's capacity is 180 Gbytes, while the RAMAC Array Subsystem stores up to 90 Gbytes. RN

IBM Storage Systems Div., Dept. P22, 5600 Cottle Rd., San Jose, CA 95193. CIRCLE 718

GRAPHICS WORKSTATION SUPPORTS COLOR IMAGING APPLICATIONS

A new graphics subsystem is available with the SparcStation 5 workstation. The 24-bit graphics solution, called the S24, is aimed at color document imaging, graphics design and color publishing, medical imaging, and multimedia. The new platform is designated the SparcStation 5S24. The S24 technology is incorporated directly on the SparcStation's high-speed memory bus (180 Mbytes/s) to take advantage of the microSparc II processor.

The graphics adapter actually sits on a mezzanine card that plugs into the SparcStation's system board. The card contains a frame-buffer controller, a RAM, video RAM, and a dynamic RAM. It offers multiple 24-bit modes, such as true color, direct color, linear color, and 8-bit indexed mode, and supports simultaneous display of 16.7 million colors and 1152-by-900-pixel resolution at 76 and 66 Hz.

The low-cost SparcStation 5S24 holds from 16 to 256 Mbytes of RAM. Internal storage ranges from 535 Mbytes to 2.1 Gbytes. With the accelerated graphics, it can supply 307,000 24-bit 2D vectors/s. The base configuration, with 16 Mbytes of DRAM, a 17-in. color display, and a 535-Mbyte hard-disk drive, sells for $6595 and is available now. Users of existing systems can upgrade to the S24 graphics for $1500.

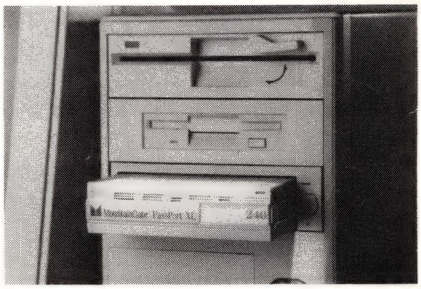
Sun Microsystems Computer Corp., *2550 Garcia Ave., Mountain View, CA 94043; (800) 872-4786.* CIRCLE 719

■ *RICHARD NASS*

RUGGED 170-MBYTE DRIVE FITS PCMCIA SLOT

The EHDD170 drive is an example of the downsizing of form factors. The PCMCIA Type II form-factor drive holds 170 Mbytes of data. Its rugged case design lets it withstand 750 G of impact. The drive offers a data-transfer rate of up to 3.5 Mbytes/s. It also boasts a track-to-track seek time of 2 ms and an average seek time of 12 ms. In full-power (read or write) mode, the drive consumes from 1.9 to 2.5 W. In sleep mode, the consumption drops to 5 to 25 mW. Available now, the EHDD170 170-Mbyte PCMCIA disk drive is priced at $629. RN

Epson America Inc., 20770 Madrona Ave., Torrance, CA 90503; (800) 289-3776 or (310) 782-0770. CIRCLE 720



RAID HITS DESKTOP PCS WITH REMOVABLE DRIVE

Using disk-mirroring software, the PassPort XL family of 3.5-in. removable disk drives can feature a RAID capability. This quick and easy way to safeguard critical data is handled through a RAID Level 1 technique to back up as much as 1 Gbyte of data. The key feature of the software is its continual maintenance of an identical copy of the primary drive to the secondary drive. It is DOS- and Windows-compatible, including Windows for Workgroups and other DOS-based peer-to-peer networks. And the removable drive, which ranges in capacity from 170 Mbytes to 1 Gbyte, can be swapped to archiving purposes. The drive offers a 9.5-ms average access time and a boot-switch capability that lets the PassPort XL serve as the primary drive. Available now, the 1-Gbyte unit sells for $1950. The disk-mirroring software costs $499. A docking station with a host adapter for an internal configuration is available and priced at $529. RN

MountainGate Data Systems Inc., 9393 Gateway Dr., Reno, NV 89511; (800) 556-0222 or (702) 851-9393. CIRCLE 721

BEHAVIORAL SIMULATION SYSTEM SIMPLIFIES AND SPEEDS ANALOG AND MIXED-SIGNAL DESIGN

Engineers creating analog and mixed-signal systems can speed up their work with a top-down analog design environment that uses behavioral simulation. SpectreHDL, from Cadence Design Systems, is a dual-language analog behavioral-simulation system. The two languages are commercial versions of VHDL-A and Verilog-A, the proposed industry-standard analog extensions to the standard digital hardware-description languages. SpectreHDL simplifies analog-model development, and speeds analog and mixed-signal simulation by up to 100 times, depending on the behavioral modeling level that's used.

The SpectreHDL engine and environment accepts VHDL-A, Verilog-A, and Spice net lists. In addition, SpectreHDL has a flexible architecture that can accommodate evolving standards. This ensures that users' investment in analog model libraries will be preserved as language standards are refined.

SpectreHDL is integrated into the Cadence Analog Artist and Analog Workbench design systems, which provides a complete front-to-back top-down design flow for analog and mixed-signal products. The integration ensures consistency from a high-level view of a design down to physical layout. Design-parameter constraints and design-consistency information automatically propagate down through the design hierarchy.

The environment has a familiar Spice-like schematic-entry system that lets users mix Spice schematics with language blocks. For example, engineers can choose to add just a few analog behavioral blocks to a Spice schematic, or they can enter behavioral representations entirely in language using an integrated text editor.

Analog-model development is made easier with SpectreHDL and the Resolve Optimizer. The two provide an automated extract-simulate-optimize loop that simplifies and speeds creating models.

In IC design, for instance, the automated loop starts by extracting RC parasitics from a rough physical layout of the target block. It then selectively back-annotates the parasitics to an accurate transistor-level model that serves as the Spice reference circuit for the block. By comparing the simulation results from the reference circuit and the initial behavioral model, the Cadence Resolve optimizer automatically adjusts selected AHDL model parameters to drive the model results to match those of the reference circuit. Using this technology, AHDL model accuracy can be within 1-2% of reference-circuit accuracy.

Good modeling practice with SpectreHDL can produce three to four levels of analog behavioral modeling for each block in a design. High simulation speed is then obtained by using high-level models for most of the blocks, and low-level models for a few of the blocks where detailed circuit behavior needs examination.

Cadence claims that simulation speed up of more than two orders of magnitude is possible with the Spectre mixed-level approach. For example, on an oversampled delta-sigma a-d converter that requires millions of simulation time points, the simulation would run for weeks at the Spice level. A meaningful behavioral-level simulation can be run in less than 90 seconds using SpectreHDL.

SpectreHDL supports multi-disciplinary system simulation, including electrical, electro-mechanical, thermal, and optical analysis. This capability is available for both VHDL-A and Verilog-A. It also accepts linear, nonlinear, and dynamic modeling. Because modules instantiate as a Spectre net-list primitive, it's simple to mix AHDL blocks with a Spice description.

The first release of SpectreHDL includes a dual-language AHDL engine, and a language compiler for both Verilog-A and VHDL-A modeling. It's available now as a stand-alone product, or as an option to the company's Analog Artist and Analog Workbench environments. List price starts at $10,000, and requires an underlying Spectre simulator.

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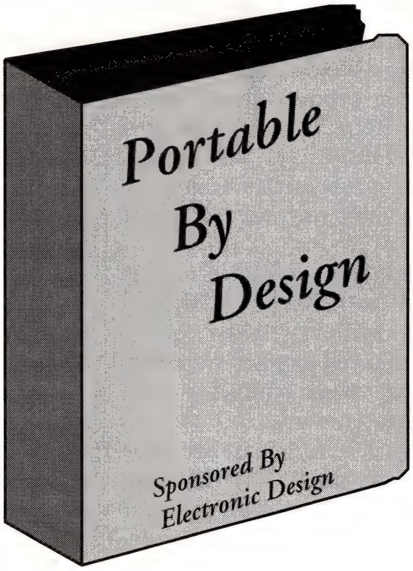

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UPCOMING MEETINGS

SEPTEMBER

IEEE International Symposium on Compound Semiconductors, Sept. 18-22. Del Coronado Hotel, San Diego, CA. Contact James Harbison, Bellcore, 331 Newman Springs Rd., Room 3X-211, Red Bank, NJ 07701; (908) 758-3386; fax (908) 758-4372.

14th IEEE International Semiconductor Laser Conference, Sept. 19-23. Hyatt Regency Maui, Maui, HI. Contact Samantha H. Phillips, IEEE/LEOS, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331; (908) 562-3894; fax (908) 562-1571; E-mail: s.phillips@ieee.org.

ASIC Conference and Exhibit (ASIC '94), Sept. 19-23. Rochester Riverside Convention Center, Rochester, NY. Contact Paul P.K. Lee, Eastman-Kodak Co., Rochester, NY 14650-2008; (716) 477-2869; fax (716) 477-4947.

AUTOTESTCON '94, Sept. 20-22. Disneyland Hotel, Anaheim, CA. Contact Robert Rassa, ManTech International, 150 S. Los Robles Ave., Suite 350, Pasadena, CA 91101; (818) 577-7100; fax (818) 577-7102.

Embedded Systems Conference, Sept. 20-23. Santa Clara Convention Center, Santa Clara, CA. Contact (415) 905-2354 for more information.

Canadian Conference on Electrical and Computer Engineering, Sept. 25-28. World Trade & Convention Centre, Halifax, Nova Scotia. Contact C. Baird, Dept. of Electrical Engineering, Technical University of Nova Scotia, P.O. Box 1000, Halifax, Nova Scotia, B3J 2X4 Canada; (902) 420-7717; fax (902) 422-7535.

2nd IEEE Workshop on Interactive Voice Technology for Telecommunications Applications, Sept. 26-27. Sumitomo Hall, Kyoto, Japan. Contact Sadaoki Furui, NTT Human Interface Labs, 3-9-11 Midori-cho, Musashino-shi, Tokyo, 180 Japan; 81-422-59-3910; fax 81-422-60-7808.

WESCON '94, Sept. 27-29. Anaheim Convention Center, Anaheim, CA. Contact Joan Carlisle, Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045; (310) 215-3976; fax (310) 641-5117.

3rd International Conference on Universal Personal Communications, Sept. 27-Oct. 1 (ICUPC '94). San Diego, CA. Contact Henry A. Macchio, Hughes Network Systems Inc., 10450 Pacific Center Ct., San Diego, CA 92121; (619) 452-4610; fax (619) 597-8979.

OCTOBER

MILCOM '94, Oct. 1-5. Fort Monmouth, NJ. Contact Donald L. Schilling, InterDigital Communications Corp., 85 Old Shore Rd., Suite 200, Port Washington, NY 11050; (516) 883-0760; fax (516) 883-0746.

1994 IEEE International Test Conference (ITC), Oct. 2-6. Sheraton Washington Hotel, Washington D.C. Contact Doris Thomas, International Test Conference, 205 Tennyson Ave., Suite C, Altoona, PA 16602; (814) 941-4666; fax (814) 941-4668.

Antenna Measurement Techniques Symposium '94, Oct. 3-7. Hyatt Regency, Long Beach, CA. Contact James P. McKay, The Aerospace Corp., M1/135, P.O. Box 92957, Los Angeles, CA 90009; (310) 336-1596; fax (310) 336-6225.

Far East Tour 1994, Electronics & Computer Shows, Oct. 4-17. Japan, Taiwan, Hong Kong, Korea, China, Singapore. Contact Ellen Wong, Commerce Tours International Inc., 870 Market St., Suite 920, San Francisco, CA 94102; (415) 433-3072; fax (415) 433-2820.

CD-ROM Expo/Boston, Oct. 5-7. World Trade Center, Boston, MA. Contact Mitch Hall & Associates at (617) 361-2001.

3rd International Exhibition of Computer & Applications for China-Shanghai, Oct. 6-10. Shanghai Centre, Shanghai, China. Contact Ellen Wong, Commerce Tours International Inc., 870 Market, St. Suite 920, San Francisco, CA 94102; (415) 433-3072; fax (415) 433-2820.

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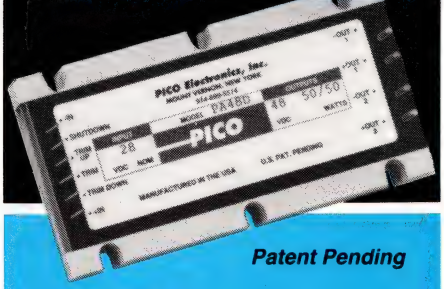

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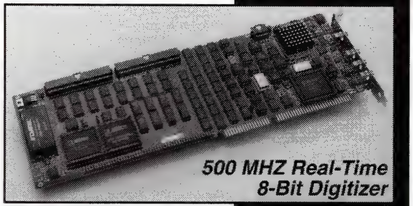

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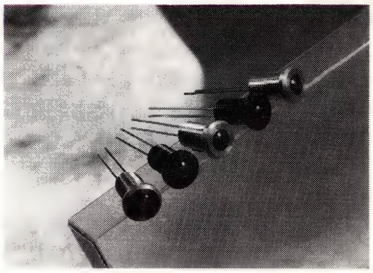

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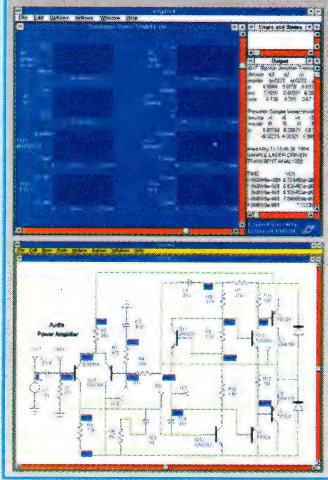

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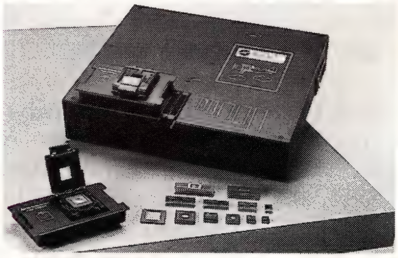

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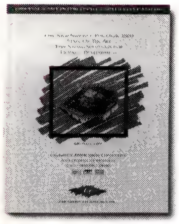

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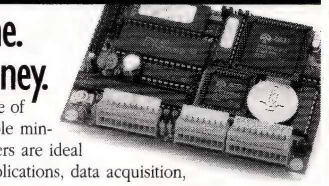

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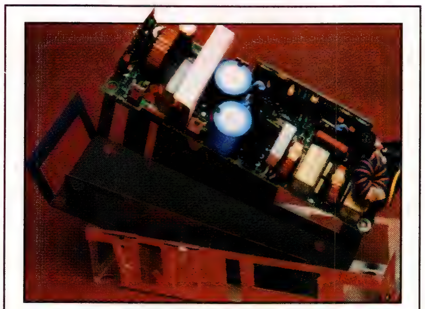

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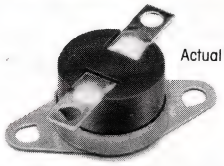

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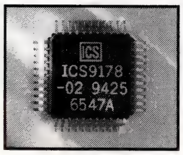

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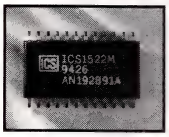

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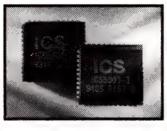

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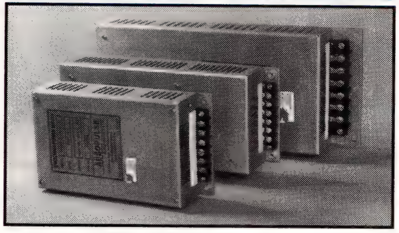

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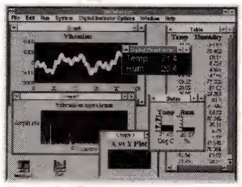

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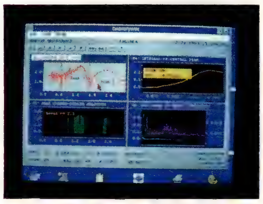

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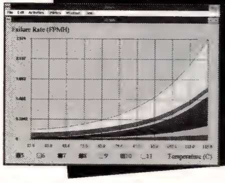

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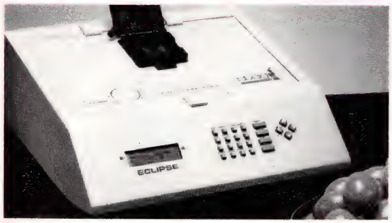

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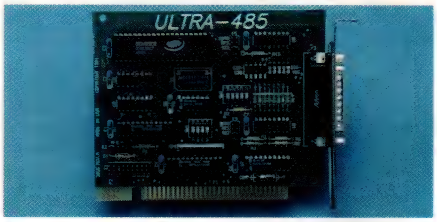

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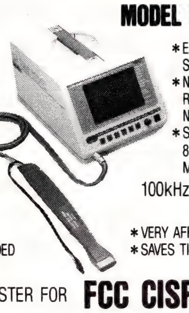

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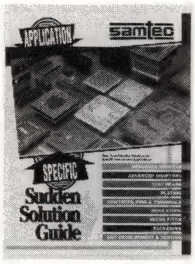
APPLICATION
samtec
SPECIFIC
Sudden Solution Guide

Literature from Samtec, New Albany, Ind., describes capabilities for developing interconnects for specific customer applications. Many standard company interconnects and most company manufacturing capabilities lend themselves to modification and optimization of customer board designs.

Samtec's capabilities include interstitial and SMT PGA sockets, smart sockets, BGA sockets and adaptors, standard and custom footprint chip adaptors, test heads and custom pins, insulators, and plating. An SMT lab also is available for customer development and testing. CM

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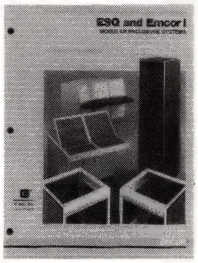
CATALOG COMBINES ESQ, EMCOR I ENCLOSURES

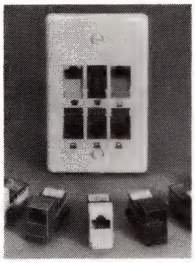

ESQ and Emcor I

Emcor Products, Rochester, Minn., has combined its popular ESQ and Emcor I modular enclosure systems into one easy-to-use catalog. The two product lines share many design, dimensional, and structural characteristics while featuring unique styling differences. Emcor's ESQ line of enclosures offer a popular squared appearance, while Emcor I frames and side panels are rounded to provide a softer look when desired.

Both the ESQ and Emcor I products have been expanded to include the other's most popular features. New options for ESQ include 30-in. panel-width frames and redesigned lower-cost wedge units; Emcor I products offer 30-3/4-in.-deep frames and new window door options.

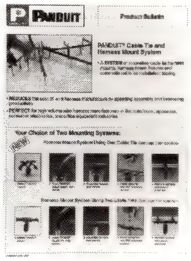
The ESQ and Emcor I product lines are fully modular enclosure systems, offering unlimited console configurations and a large variety of component accessories. The free 72-page, color catalog contains an easy ordering guide. CM **CIRCLE 628**

MODULAR JACKS COME IN COLORS



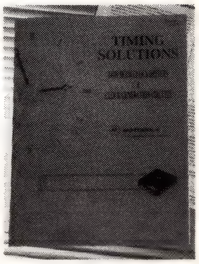
PAN-JACK Category 5 modular jacks are available in 11 colors from Panduit Corp., Network Systems Division, Tinley Park, Ill. The colors give the user an easy means for custom port identification and can also be used to complement the decor of the premises. PAN-JACK modular jacks terminate 22-24 AWG unshielded twisted pair and are designed to accept two-, three- and four-pair plugs. Insulation displacement contacts provide quick, reliable termination. The clear, removable termination cap securely retains wires, provides excellent strain relief, and facilitates troubleshooting. Twists are maintained to within 0.5 in. to meet Category 5 installation requirements. The colored modular jacks are part of a full line of network wiring products. CM **CIRCLE 629**

BULLETIN DESCRIBES HARNESS MOUNT SYSTEMS


PANDUIT
Product Bulletin

A free bulletin from Panduit Corp., Electrical Group, Tinley Park, Ill., describes the company's wire harness-mount system. The system is designed to reduce the cost of high-volume wire-harness manufacturing. The four-page, illustrated bulletin features Panduit's push and screw-mount fasteners, and the company's corresponding harness-board fixtures. These mounts are designed to be secured to wire harnesses via Panduit's semi- and fully automatic cable tie equipment. Product listings are provided in tabular form, giving part numbers, dimensional drawings, and application specifications. Also included is information regarding the company's cable tie installation equipment for standard and miniature cross-section cable ties. The harness-mount systems are part of a complete line of wiring products. CM **CIRCLE 630**

TIMING SOLUTIONS DATA BOOK


TIMING SOLUTIONS

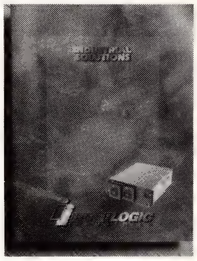
The Motorola Timing Solutions Data Book (BR1333/D) from Motorola, Phoenix, Ariz., is aimed at designers who need to distribute clock signals. This 190-page book includes what the company cliams is the industry's broadest offering of clock distribution circuits with timing solutions spanning all logic technologies—TTL, CMOS, ECL, PLL, biCMOS, and others.

Revision 3 has been expanded to contain all of the latest information on Motorola's low-voltage PLL clock drivers, 5-V PLL clock drivers, low-voltage/low-skew fan-out buffers, low-skew fan-out buffers, and clock-generation circuits.

Data sheets, as well as application-notes section on system-design considerations, clock-distribution techniques, and designing with PECL are included.

For a free copy of the data book, call Motorola Literature Distribution at (800) 441-2447, or (602) 994-6561 outside of the U.S. CM **CIRCLE 631**

ISA/IBM AT PACKAGING HANDBOOK



Interlogic Industries, Melville, N.Y., has released its 1994 ISA, EISA & VESA packaging handbook for single-board computers, passive backplanes, and industrial enclosures. The brochure contains a complete list of single-board computers from the 286 through the 486DX2 66-MHz version. The catalog lists all of the comprehensive specifications that a design engineer would need to choose a single-board computer, along with the packaging that will be required. The company supports its product line with a complete line of industrial rack-mount chassis, micro towers, display monitors, rack-mount keyboards, and EL display rack-mount computers. CM **CIRCLE 632**

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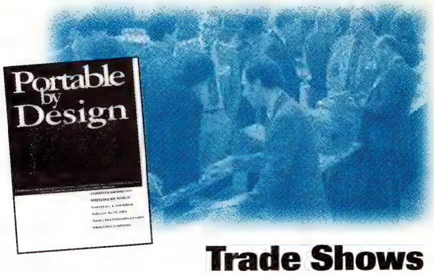

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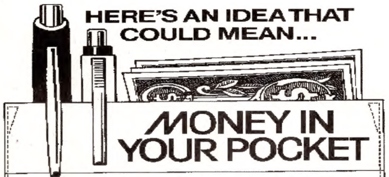
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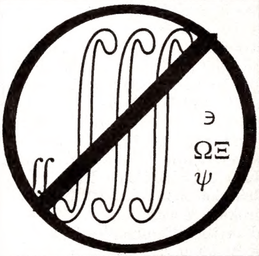

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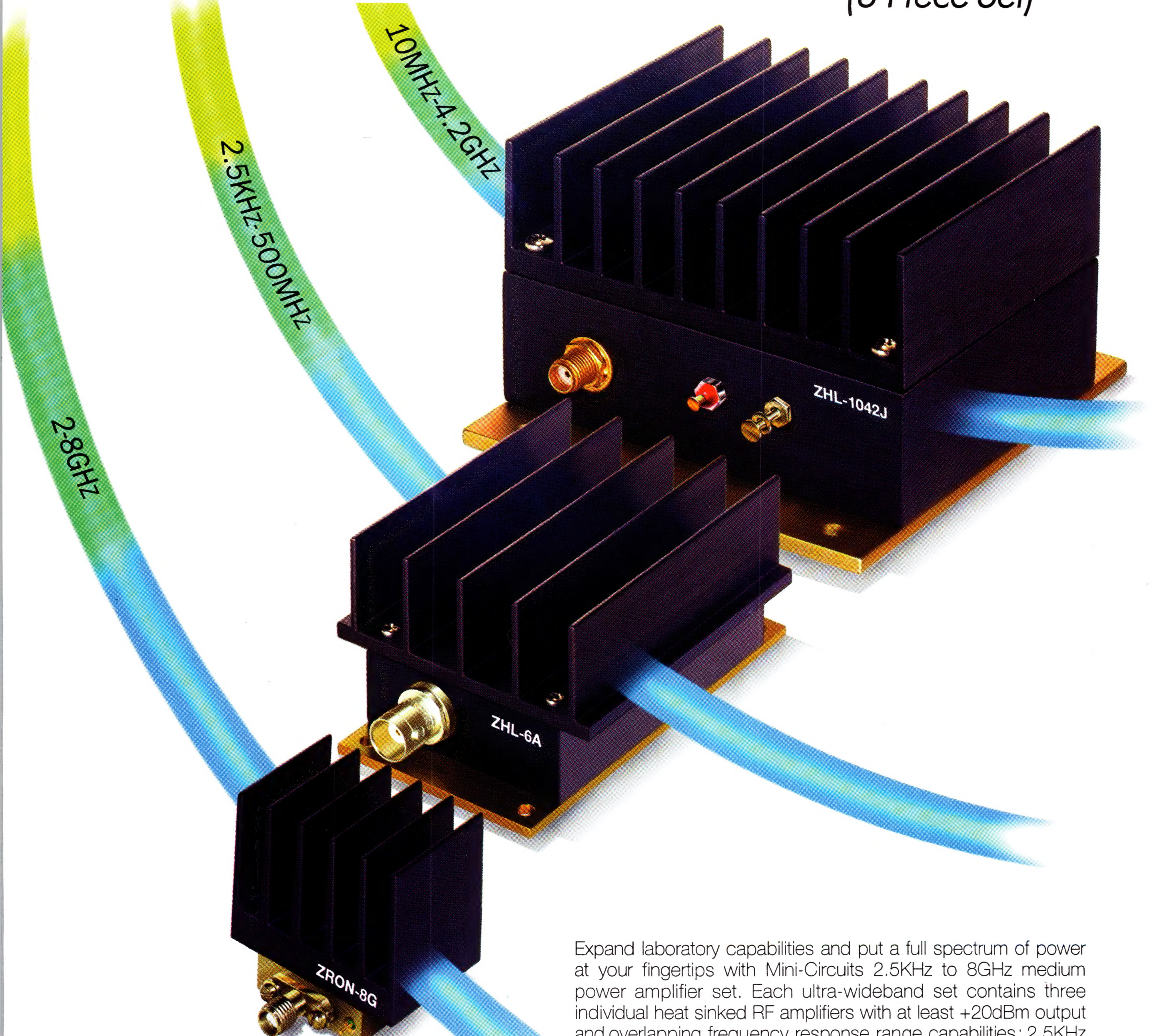

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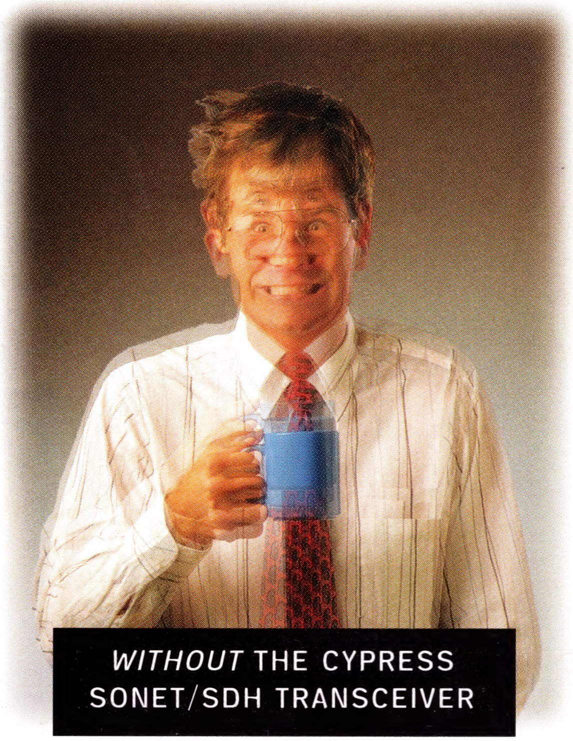

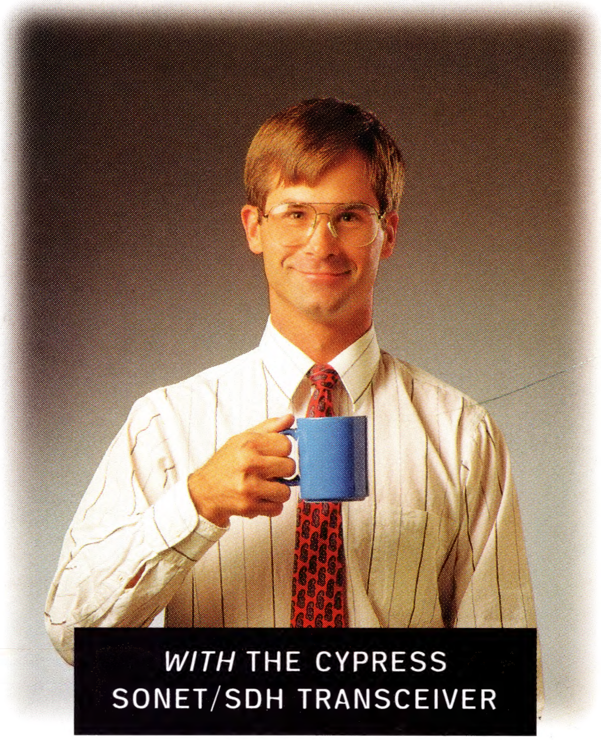

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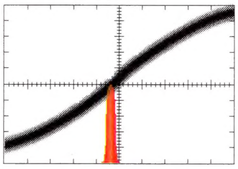

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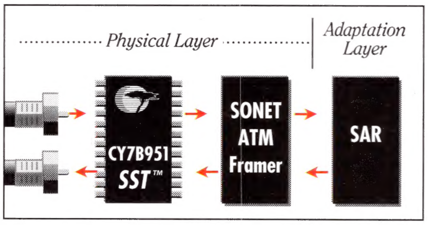

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